A HW/FW Co-Designed SSD Controller Architecture to Boost up SSD Performance

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Explosive NAND IF Bandwidth

- ONFI1.0: 50MB/s
- ONFI2.0: 133MB/s
- ONFI2.1: 200MB/s
- ONFI3.0: 400MB/s
- ONFI3.2: 533MB/s
- ONFI4.0: 800MB/s
- ONFI4.1: 1200MB/s

x 60
Client SSD Trend

- **SATA3 6Gb/s**
- **ONFI1.0**: 50MB/s
- **ONFI2.0**: 133MB/s
- **ONFI2.1**: 200MB/s
- **ONFI3.0**: 400MB/s
- **ONFI3.2**: 533MB/s
- **ONFI4.0**: 800MB/s
- **ONFI4.1**: 1200MB/s

- **PCIe Gen3x4 32Gb/s**: x 5
- **PCIe Gen4x4 64Gb/s**: x 2
SSD Performance Issue

Performance vs. NAND Die #

- Host IF Limit
- Sequential Performance
- Random Performance Limit
- Random Performance

Huge Gap!
Bottleneck of SSD Performance

Heavy FW Workloads

CPU Sub-System

Host

Host Controller

Data Buffer

Flash Controller

NAND
Details of CPU Workloads

- Typical solution: Increasing CPU cores
  - More CPU partitions
  - Complicated FW architecture
  - Low power efficiency

Heavy CPU workload

SSD Performance

CPU Core #

NAND CMD Scheduling
FTL Management
CMD Translation
Buffer Management
Host CMD Protocol

[Graph showing SSD Performance vs. CPU Core #]

Flash Memory Summit 2019
Santa Clara, CA

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Cross-Layer Design Methodology

- HW/FW Co-designed architecture to offload CPU
  - Seamless FW/HW flow
  - Simple FW architecture
  - High power-efficient
Unified HW/FW Data Structure

- HW/FW Shared data structure (e.g., descriptor), containing all information about the atomic data unit managed by FW.
- HW automation for descriptor pool management, including descriptor allocation/release and queue management.
Virtual Buffer Management

- Physical buffer segments shared by virtual buffers
  - Virtual buffers are defined by FW
  - HW automation of buffer allocation/release

- Virtual buffer attributes
  - Buffer ID
  - Min/max size
  - Buffer allocation policy
Maxio NPU Technology

- Private instruction set for NAND flash memory
  - Flexible NAND command sequence
  - Support NAND models of all NAND vendors

- Specified NAND Processing Unit (NPU) architecture - NPU
  - Support multiple thread
  - HW automation of thread interleaving
  - NPU core: 4 pipeline stages for high speed NAND IF
## Maxio MAP1001 Performance Result

### Flash Memory Summit 2019
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<thead>
<tr>
<th>Configuration</th>
<th>Random Read</th>
<th>Random Write</th>
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<tr>
<td>8CH x 1CE</td>
<td>217K</td>
<td>305K</td>
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<tr>
<td>8CH x 2CE</td>
<td>360K</td>
<td>546K</td>
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<tr>
<td>8CH x 4CE</td>
<td>672K</td>
<td>616K</td>
</tr>
<tr>
<td>8CH x 4CE x 2LUN</td>
<td>&gt; 800K</td>
<td>607K</td>
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<table>
<thead>
<tr>
<th>Configuration</th>
<th>Read [MB/s]</th>
<th>Write [MB/s]</th>
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<td>8CH x 4CE x 2LUN</td>
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</tbody>
</table>
Thank you!

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