RaW Access to Flash Memory (Meets Special Needs)

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Static RAM does not need a refresh controller

However, for Flash (static) Memory a controller for Flash Translation Layer and other control functions has become pervasive

Open Channel reduces control in mem device

Could there be an opportunity for more simple direct access to such static memory?
The Controller Argument

• The various architectures of Flash Memory (S/M/T/QLC) and its use for file storage has required a Controller to provide transparent access to the memory as for disk systems.

• Apparently, Eli Harari (Sundisk) early-on recognized the need for a “Controller” to manage the Flash memory arrays and also perform many auxiliary functions. [1]
Controller Functions

- The Controller performs functions such as:
  - Logical to Physical address translation
  - Allocation
  - Garbage Collection
  - Wear Levelling
  - Error Correction
  - Periodic Data Retention moves
The Subsequent Argument

- Where should the Control functions reside:
  - In Memory Subsystem (HW or programmable)?
  - Or External (Software or Hardware) in Host?
  - Or Hybrid? (part in Host, part in Mem Subsystem)

- With increased use, there has been growing demand for more direct access to memory

- Amount and location of Control functions are then left to the system designer/implementer
• Symphonic Cooperative Flash Management [3]
• Observed latency spikes issue in RW cycles
• Some attempted to fix by (large write) stripes
• Radian “cooperative” Symphonic CFM fits in: FTL <-> Hybrid CFM <-> Host Managed RAW
• Host User program controls function in device
• Hides device details whilst allow user control
Multi Level characteristics

- SLC: $2 V_{TH}$ for 2 states (0 1) store 1 bit
- MLC: $4 V_{TH}$ for 4 states (00 01 10 10) store 2 bit
- Multiple $V_{TH}$ (Voltage Thresholds) for multiple bits on same cell reduces gap between adjacent voltage ranges which define the thresholds
  - Small gap more prone to errors: therefore requiring ECC
  - Increased access to same cell results in increased wear: thereby requiring control functions to move data around
- Multi bit on 1 Floating Gate = no single bit access
Propose HW Programmable Option

- Hardware programmable options are common in digital logic hardware controllers
- Memory chipsets are more limited and rigid in what they present to the system designer
- The Proposal is to petition flash memory chip manufacturers to provide a programmable option for direct RaW Access mode
RaW Access mode option

Control (to support RaW Access mode)

Address

Data

Flash Memory Chip
Or Subsystem
(any Control function should be User Programmable)

BUS can be parallel or serial
Toshiba 8Gb NAND TH58xxx

• 4224 bytes x 64 pages x 4096 blocks
• Read in 4224 bytes (1 page) increments
• Erase operation implemented in single block unit: 4224 bytes x 64 pages
• App note provides that NAND Management such as Bad Block Management, ECC treatment and Wear Leveling should be incorporated in the system design [4]
Toshiba 8Gb NAND TH58xxx cont.

• ECC logic on-chip; not programmable
• MODES: Read, Reset, Auto Page Program, Auto Block Erase, Status Read, Page Copy, Multi Page Read, Multi Page Program, Multi Block Erase, ECC Status Read
• Access Times:
  • Read (13.2 us/page, 25ns/cycle)
  • Auto Page Program (340 us/page includes read verify)
  • Auto Block Erase (2500 us/block)
• Petition to add **RaW Access** mode via supporting new hex value Commands for:
  • NO ECC
  • Single Page Erase?
  • Operate TLC in SLC mode? Samsung 840 EVO
  TLC reserves a portion of the die as SLC cache \[5\]
  • Individual bit access if multiple floating gates?
• Backward pin-compatible!
Analysis

• Pros
  • Design flexibility
  • Potential for increased access speed

• Cons
  • Requires HW rework first time round
  • Speed versus Density tradeoff
Benefits

• For high volume deployments any cost reduction aggregates into significant saving
• Implementation of any required control functions in software provides Nick McKeown’s “Software-Defined” capability
• Less hardware logic implemented in chip results in smaller die size hence lower cost
Acknowledgements


• [4] Toshiba TH58BVG3S0HTA00 NAND EEPROM

Q & A