Challenges of Testing PCIe Gen. 4 SSDs and Beyond

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Agenda

- MPT3000 SSD Tester
- Implementing PCIe Gen. 4 Early
- Specification Issues
- Testing Issues
- Test Compliance Issues
- PCIe Gen. 5 and 6
- SAS-4 and SAS-5
Our PCIe Gen. 4 Product

• The MPT3000 is a multi-protocol SSD tester
  • FPGA based implementation allows for the protocol switches
Risking Early Development

- Hardware developed for the 0.7 physical layer of the PCIe Gen. 4 specification
- By using the FPGA we were able to test before the Gen. 4 devices became available
Testing the Link

• No devices to test the link available
  … so we made our own
  ▪ To be an early adopter you need to build your own test equipment

• Test board has many debug features to test the link
Eye Diagram

- Eye Diagram tool added to debug the link
  - Similar to Rx Margin (a.k.a. Lane Margining)
- Adding eye diagram to SSD controllers is suggested
Changes to the Specification

• The optional lane margining feature was made mandatory at the last moment … surprise

• Causing implementation mismatch requiring rearchitecting
  • Budget time and resources for specification changes
Testing the Performance

• No SSD available to test with … so we made our own
• DMA transfers simulated the NVMe command
  ▪ Setting data engine speed
  ▪ Determining performance with NVMe command overhead

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PCI SIG Compliance

• Test systems were not ready
  ▪ False positives for pass and fail
  ▪ Engineering resources used to correct tests

• Test specification as of last plug fest
  • Not possible to obtain PCI SIG certification
Hurry Up and Wait

• PCIe Gen. 4 market intercept pushed out from original expectations
• Extra time allowed for feature development and stability improvements
TCDT (Traffic Capture and Debug Tool)

- Traffic Capture and Debug Tool
- Suite of user friendly graphical tools for parsing and debugging captures
- LTSSM Rules Checker
- Tools allow users to parse and analyze logs in a quick and user friendly manner
TCDT (2)

- **TLP Capture**
  - Packet capture at the TLP layer and above

- **PCIe Protocol Decoder**
  - Protocol Decoder allows the user to graphically analyze the traffic
TLP Capture Example (1)

- PCIe link framing
  - Test Log
  - Log from TLP Capture

Example of link framing failure
TLP Capture Example (2)

- No block device not ready
  - Test Log
  - Log from TLP Capture
    - NVMe controller status register CSTS.RDY reports not ready

Example of device ready failure
PCIe Gen. 5 and Beyond

- PCIe Gen. 5 is almost the same as Gen. 4
  - Early adopters will need to make their own tools
- Gen. 6 specification in 2021
  - Significant changes
    - 64 GT/s
    - Pulse Amplitude Modulation
    - Forward Error Correction
- PCI SIG on three year cycle, Gen. 7 in 2024
SAS-4 and SAS-5

- There may be a SAS-4 market … maybe
  - SAS-4 demand is limited to companies that do not want to update/upgrade databases
  - SAS optimized databases do not make good use of potential performance gains
- Will there even be a SAS-5?
Closing

- Making your own tools is crucial as an early implementor
- Starting early allows the product to mature, but is costly \( \ldots \) and frustrating
- Beware supply chain issues
  - High speed components may be in short supply
  - Resin for high speed PCBs will be costly and is in short supply
Questions?
Backup
TLP Capture Example (3)

- PCIe link rcvd_ts
- Test Log

Example of link training failure
PCIe Gen. 4 Changes

1. Speed change to 16GT/s
2. Equalization updates for 4.0 (8 GT/s to 16 GT/s)
3. TSx OS changes
4. 16 GT/s EIEOS
5. SKP OS changes (CTRL SKP)
6. Polling.Compliance update
7. 10-Bit Tag
   - Allowing for greater token count
8. Data Link Feature Exchange
9. Flow Control Scaling
10. Rx Margining (a.k.a. Lane Margining)
    - Host cabling feature
    - Pushed through as a requirement by Intel
11. Retimer
12. Configuration space register updates