Using a PCIe Analyzer with NVMe-Based Products

Isaac Livny
Teledyne Corporation
Agenda

- NVMe Command Execution
  - Host Controller Interface
  - Controller Memory Buffer
- NVMe Data Structures
  - Physical Region Page
  - Scattered Gathered List
- NVMe Analysis Engine
  - Recording NVMe transactions
  - Analysis of NVMe Events
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  - Recording NVMe transactions
  - NVMe Event capture and Analysis
NVMe command execution

1. Insert command in Queue
2. Ring Doorbell New Tail
3. Submission Queue Tail Doorbell
4. Fetch Command
5. Completion Queue Head Doorbell
6. Generate Interrupt
7. Process Completion
8. Completion Queue Head

Host Memory

Host

NVMe Controller

Submission Queue

Completion Queue

PCIe TLP

PRP / SGL
Normal mode Command execution

1. Insert command in Queue
2. Ring Doorbell
   New Tail
3. Process Command
4. Generate Interrupt
5. Queue Completion
6. Completion Queue
    Head Doorbell
7. Process Completion
8. PRP / SGL
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CMB command execution
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PRP List: points to a PRP data line
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SGL segments: SGL descriptor types
SGL descriptor rules

- Data Block Descriptor points to data payload
- Segment Descriptor points to next segment
- Last Segment Descriptor points to last segment
- Last segment cannot have a Segment or Last Segment Descriptor
- Bit Bucket descriptor has length but no pointer
SGL decode transaction layer view

1. Command line, indicating the first SGL segment for the command and decoding its fields.

2. SGL segment line decoding its fields

3. SGL data block per each SGL data block descriptor
<table>
<thead>
<tr>
<th>Device ID</th>
<th>QID</th>
<th>CID</th>
<th>Address</th>
<th>HPC</th>
<th>Fuse</th>
<th>PSOT</th>
<th>CID</th>
<th>NSID</th>
<th>PTR</th>
<th>Address</th>
<th>Type</th>
<th>Address</th>
<th>Length</th>
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<th>SLBA</th>
<th>PRIC</th>
<th>PRACT</th>
<th>VRAB</th>
<th>AF</th>
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<tr>
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</tr>
</tbody>
</table>

**Notes:**
- Santa Clara, CA
- August 2019
- Last Segment has only a Bit Bucket Descriptor
- No segment descriptor in Last Segment
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  • Recording NVMe transactions
  • Analysis of NVMe Events
NVMe Analyzer mode - Goals

- Real time analysis of NVMe products and
  - Identify specific NVMe events and scenarios
  - Identify performance bottlenecks within a long recording
- PCIe analysis engine needs to understand the NVMe command queuing mechanism
  - PCIe analysis engine self-learns queue and payload bindings
NVMe mode Long Recordings analysis

• Dropped idles, SKPs, EDSs, DLLPs and data payload
• Memory Utilization Model Assumptions
  • 16GB memory dedicated per direction
  • Capture Duration Doubles for Gen4 NVMe analyzer
• Recording stops as soon as either side fills up
• SSD rate for read is 2 GB / sec or 16 Gb/sec
  • This implies a Gen3 x4 link with 60% utilization
• Assume 16 pages / command
• Assume 2 doorbells
• Assume no interrupt aggregation
• Each TLP to occupy 1.09 to 1.43 memory blocks on average
## Recording duration using 32K DW NVMe Transfers

### Best Case
Gen 1 x1 Lane Width

<table>
<thead>
<tr>
<th>TLP size (dw)</th>
<th>100</th>
<th>90</th>
<th>80</th>
<th>70</th>
<th>60</th>
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<tbody>
<tr>
<td>32</td>
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<td>161.0213</td>
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<td>169.293</td>
<td>197.5084</td>
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<td>131.2904</td>
<td>147.7017</td>
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<td>196.9356</td>
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<tr>
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<td>117.9895</td>
<td>131.0994</td>
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<td>196.6491</td>
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</table>

### Worst Case
Gen 3 x4 Lane Width

<table>
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<th>70</th>
<th>60</th>
</tr>
</thead>
<tbody>
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<td>9.085402</td>
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<td>10.69938</td>
<td>12.48261</td>
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</table>

**Note: Capture Duration Doubles when using Gen 4 analyzer**

Santa Clara, CA
August 2019
NVMe analyzer mode

- Filter in items
  1. Entities that form NVMe Commands
  2. NVMe Control Registers
  3. PCIe entities related to NVMe traffic
  4. ACK/NAK DLLPs
  5. Interrupts
  6. PCIe configuration map

Queue allocation presents tradeoffs between memory resource allocation and data throughput.
### NVMe Analyzer mode

**Event Properties**

<table>
<thead>
<tr>
<th>NVMe Filters</th>
<th>Actions</th>
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</thead>
<tbody>
<tr>
<td><strong>Filter In (Record only these items)</strong></td>
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<tr>
<td>Controller Registers</td>
<td></td>
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<tr>
<td>CAP</td>
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</tr>
<tr>
<td>VS</td>
<td></td>
</tr>
<tr>
<td>INTMS/INTMC</td>
<td></td>
</tr>
<tr>
<td>CC</td>
<td></td>
</tr>
<tr>
<td>CSTS</td>
<td></td>
</tr>
<tr>
<td>NSR</td>
<td></td>
</tr>
<tr>
<td>AQA</td>
<td></td>
</tr>
<tr>
<td>ASQ/ACQ</td>
<td></td>
</tr>
<tr>
<td>CMBLOC/CMBSZ</td>
<td></td>
</tr>
<tr>
<td>BPINFO</td>
<td></td>
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<tr>
<td>BPRSEL</td>
<td></td>
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<td>BPMBL</td>
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<tr>
<td>DLLP ACKs</td>
<td></td>
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<tr>
<td>DLLP NAKs</td>
<td></td>
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<tr>
<td>MSI</td>
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<tr>
<td>MSI-X</td>
<td></td>
</tr>
<tr>
<td>Device Config</td>
<td></td>
</tr>
</tbody>
</table>

**Available NVMe Devices:**

```
0x00000000EF510000
```
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NVMe Analyzer mode
NVMe Analyzer mode

- NVMe Read Command Packet Level associated by queue address
  - Completion TLP with “mysterious” address field
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NVMe performance analysis

- As NVMe technology matures leading to a need to maximize performance
- What’s special about NVMe performance vs general PCIe performance
- Differences in performance analysis techniques between SSD drives and traditional magnetic drives.
NVMe latency categories

- Doorbell to command submission
- Command submission to Data transfer
- Command submission to command completion
- Command completion to interrupt
NVMe Performance management

- PCI express flow control credit starvation.
- Tradeoffs between memory resource allocation and data throughput.
- Queue allocation presents tradeoffs between command latency and throughput.
- Virtual channels manage traffic in fabric.
  - Allocate traffic classes to Virtual channels.
NVMe performance criteria

- **Response time**
  - Transmission of the complete transfer from the beginning of the PCIe packet to the end of the last PCIe packet of this NVMe command

- **Latency time**
  - Time from the last PCIe packet of the NVMe command submission to the first PCIe packet of the NVMe command completion
  - **Throughput**
    - NVMe command payload of all simultaneous coincident commands during the processing of current command divided by response time
### Instantaneous Performance Metrics

#### NVMe Cmd 21 - Read
- **Device ID**: NVMe:LeCroy000000
- **Device Name**: No frequency information provided

#### NVMe Cmd 22 - Read
- **Device ID**: NVMe:LeCroy000000
- **Device Name**: No frequency information provided

#### NVMe Cmd 23 - Read
- **Device ID**: NVMe:LeCroy000000
- **Device Name**: No frequency information provided

#### NVMe Cmd 24 - Read
- **Device ID**: NVMe:LeCroy000000
- **Device Name**: No frequency information provided
Response time

Command level metrics

Latency time

Response time
Performance Analysis via Trace Expert

- Drill down to get more reports
# Categorized Performance analysis

## Read Requests Performance

<table>
<thead>
<tr>
<th>Requester -&gt; Completer</th>
<th>Total</th>
<th>Thrp MB/s (Min)</th>
<th>Thrp MB/s (Avg)</th>
<th>Thrp MB/s (Max)</th>
<th>Resp. time (Min)</th>
<th>Resp. time (Avg)</th>
<th>Resp. time (Max)</th>
<th>Latency (Min)</th>
<th>Latency (Avg)</th>
<th>Latency (Max)</th>
</tr>
</thead>
<tbody>
<tr>
<td>00:03:00 -&gt; 00:00:00, Cfg TC0</td>
<td>416</td>
<td>0.995</td>
<td>21.175</td>
<td>1502.353</td>
<td>378.000 ns</td>
<td>1.172 us</td>
<td>3.834 us</td>
<td>204.000 ns</td>
<td>1.009 us</td>
<td>3.662 us</td>
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<tr>
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<td>5314</td>
<td>7.914</td>
<td>6189.918</td>
<td>11387.661</td>
<td>338.000 ns</td>
<td>376.760 ns</td>
<td>482.000 ns</td>
<td>174.000 ns</td>
<td>210.050 ns</td>
<td>304.000 ns</td>
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<td>7.981</td>
<td>6833.574</td>
<td>11387.661</td>
<td>338.000 ns</td>
<td>382.470 ns</td>
<td>478.000 ns</td>
<td>174.000 ns</td>
<td>216.120 ns</td>
<td>304.000 ns</td>
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<td>1044</td>
<td>0.245</td>
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<td>1526.181</td>
<td>2.522 us</td>
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<td>302.000 ns</td>
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Timing Calculator Queue View

- View submission and completion Queues
- Compare Queues to see where overloading is occurring
- Verify if submission and completion queues are equal and that nothing was lost
NVMe Command IOPS Statistical Information
Trigger on doorbell latency > 3 msec
Conditional performance analysis using Verification scripting

- Extract metrics within a defined range
- LBA drive access pattern
- Queue access distribution
- Low power states entry / exist
- Multiple NVMe commands per TLP referenced by time stamps
VSE script example

```c
OnStartScript() {
  ReportText("OnStartScript called...");
  ReportText("\n\nRunning...\n");
  EventCount = 0;
  SendAllChannels();
  SendAllTraceEvents();
  #SendLevelOnly( _NVMC );
  #SendLevelOnly( _SPLIT );
  #ScriptForDisplayOnly();
  # Comment the line below - if you want to enable output from ReportText()-functions.
  DisableOutput();
  filePtr = OpenFile("C:\Documents\test.csv");
  WriteString(filePtr,"Start time, Response time, latencyTime, LBA, Length, QID, FUA");
}
ProcessEvent() {
    respTime= in.Metric_ResponseTime;
    latencyTime=in.Metric_LatencyTime;
    time=in.Time;
    throughput=in.Metric_Throughput;
    CMD = in.nvmCommandOpCode;
    NLB = in.Read_NLB;
    SLBA0 = in.Read_SLBA_DW0;
    SLBA1 = in.Read_SLBA_DW1;
    SLBA = in.Read_SLBA;
    SQID = in.nvmcSubmissionQueueID;
    if( CMD!= 1 ) FUA = 0; else FUA = in.Write_FUA;
    if (SQID!= 0) { ReportText(FormatEx("%s,%s,%d,%s,%d,%d,%d",CSV_Val_TimeStamp_Seconds(in.Time ),
                                      CSV_Val_TimeStamp_Seconds(respTime), CMD, (SLBA), (NLB+1), SQID, FUA));
            WriteString(filePtr,FormatEx("%s,%s,%s,%s,%d,%d,%d",CSV_Val_TimeStamp_Seconds(in.Time ),
                                        CSV_Val_TimeStamp_Seconds(respTime),CSV_Val_TimeStamp_Seconds(latencyTime),
                                        (SLBA), (NLB+1), SQID, FUA)); } 
    if( EventCount == MAX_NUMBER_OF_EVENTS ) ScriptPassed(); EventCount++; return Complete(); }
SSD traffic statistics

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<tr>
<th>Start time</th>
<th>Response time</th>
<th>Command</th>
<th>LBA</th>
<th>Length</th>
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</table>
NVMe Analyzer mode summary

- Keep only NVMe transactions
  - Link layer and physical layer traffic truncated
  - PRP/SGL Data payload truncated
- NVMe transactions selectively included
- Long recordings made possible
- Enables utilization of advanced metrics
  - Trap long latency events