STT–MRAM: High Density Persistent Memory Solution

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MRAM Brings Native Persistence to Memory Workloads

- **Non-Volatile**: Maintains data without power or refresh
- **Fast**: Read/write similar to DRAM
- **Endurance**: Handles memory workloads

MRAM combines performance of memory with persistence of storage.
Everspin STT-MRAM in Production

- **256Mb ST-DDR3 MRAM**
  - 40nm CMOS
  - 1.5V DDR3 VDD/VDDQ
  - Standard JEDEC DDR3 ball configuration

- **1Gb ST-DDR4 MRAM**
  - 28nm CMOS
  - 1.2V standard DDR4 VDD/VDDQ
  - Standard JEDEC DDR4 ball configuration
STT-MRAM – Easy to Integrate with Standard CMOS

Off Axis Integration, 256Mb

On Axis Integration, 1Gb

MRAM Layer Additions

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Free Layer Engineering for STT Efficiency

- Free layer designs with different materials
  - Lower $V_c$ and higher $E_b$ indicates better STT switching efficiency
  - Figure of Merit for product efficiency and reliability is: $E_b(105 \ C) / V_c(20 \ C)$
- Each series is a range of thickness
- $E_b$ is flat but $V_c$ varies for a range of thickness near the optimum $E_b$ design point
- $E_b$ increased $\sim 35\%$ with $<5\%$ increase in $V_c$ from lowest to highest $E_b$ design
Materials Design for Scaling

- Data retention bakes at 160°C
- Data retention flips measured for 4 nominal bit sizes and fit to obtain $E_b$
- $E_b$ decreases linearly with bit diameter
- Magnitude of $E_b$ is tunable through free layer design
The field switching distribution correlates to the resistance to thermal fluctuation

The large separation from 0 field indicates essentially zero probability of spontaneous flips
Better Margin for Manufacturability

- Error rates < 1E-6 (raw bit error rate) achieved for both 256Mb and 1Gb
  - Relative Vswitch of > 1.5 for 256Mb and > 1.4 for 1Gb
  - Improved (narrower) distribution in both directions going from 256Mb to 1Gb
Zero fails for range of write pulse widths ≥ 10-12 ns for 256Mb and ≥ 6-8 ns for 1Gb
- Endurance is better with longer pulses due to the lower required write bias
- Clock rate is not affected by the choice of pulse width in this range

Improved switching efficiency for 1Gb enables better performance
- Full array cycling with stress to accelerate fails
  - Used bias and temperature acceleration to predict endurance at operating conditions
  - Product endurance >1E10 cycles to BER specification is demonstrated

- Improved extrinsics for 1Gb (linear down to -14 on Weibull scale)
Widening Operating Temperature Range

- Baked parts at elevated temperature to accelerate fails
  - Free layers engineered to achieve desired data retention
- 10yr @ 85C data retention achieved for 1Gb parts with 1e10 endurance
Everspin has successfully transitioned STT-MRAM from R&D to volume manufacturing.

STT-MRAM is approaching DRAM Density and Feature Size:
- Switching efficiency improvements for STT-MRAM expected to scale with bit size enabling

Source for SRAM, DRAM, NAND:
The International Technology Roadmap for Semiconductors
The International Roadmap for Devices and Systems
Acknowledgements

- Colleagues at Everspin Technologies:

- Partners for STT-MRAM Manufacturing & Development
Thank you.