Update XP ReRAM Technology

Amigo Tsutsui
Sony Semiconductor Solutions Corp
Cross Point ReRAM

ReRAM
- Mechanism: Conductive Bridge type
- Program: 50uA
- On/Off state: LRS Low R State ~10kohm, HRS High R State >10Mohm
- Endurance: 1M cyc
- Retention: >10 yrs @55C
- Scaling: Confirmed down to 10nm

Selector
- Mechanism: OTS (Ovonic Threshold Switch)
- On/Off current: 50uA / ~5nA@75% bias
- Endurance: 100M cyc
- Scaling: Confirmed down to 10nm
Memory Cell IV-Curve

ReRAM + Selector = 1S1R

- Set
- Reset
- HRS
- LRS
- Snapback
- Isnap
- Vsnap
- Off region by selector
Memory Cell Operation

Selector: Off $\rightarrow$ On
ReRAM: LRS $\rightarrow$ HRS (Reset)

Selector: Off $\rightarrow$ On
ReRAM: Stay LRS

Selector: Off $\rightarrow$ On
ReRAM: HRS $\rightarrow$ LRS (Set)
Care for Drift on Margins

Santa Clara, CA
August 2019

ReRAM: LRS (Low Resistance State)
ReRAM: HRS (High Resistance State)

Voltage (V)

Set Window
Read Window
Reset Window

Read fail
Set fail
Reset fail

Vreset
0V
Vread
Vset

Negative bias
Positive bias
## Read-induced Overset

<table>
<thead>
<tr>
<th>ReRAM LRS</th>
<th>Data</th>
<th>Effect</th>
</tr>
</thead>
<tbody>
<tr>
<td>Weak Set ~100Kohm</td>
<td>0 or 1</td>
<td>Somewhere in between HRS and LRS due to poor set. This failure can be detected by voltage sense amp.</td>
</tr>
<tr>
<td>Normal Set ~10Kohm</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>Overset ~Kohm</td>
<td>1</td>
<td>Deeply overset by multiple read stress which lead to Reset failure. Prevention scheme such as “Reset and Set after multiple read” is needed.</td>
</tr>
</tbody>
</table>
Summary

• Need a special controller technology
  • Selector Drift
  • Read-induced overset