Component-Level Characterization of 3D TLC, QLC, and Low-Latency NAND Component-Level Characterization of 3D TLC, QLC, and Low-Latency NAND

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Agenda

Importance of 3D QLC

Characterization of 3D QLC

Characterization of 3D TLC

Characterization of Low-Latency NAND

3D TLC, QLC, and Low-Latency NAND Characterization

Importance of 3D NAND Characterization
Importance of 3D NAND Characterization

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Component-level characterization of 3D NAND is essential for end-use applications. IBM FlashSystem leverages extensive component-level characterization that closely matches expected use-cases.

3D NAND presents characterization challenges—but also opportunities. Characterization that closely matches expected use-cases is the most valuable. Many avenues for optimization exist for 3D NAND characterization. Component-level characterization of 3D NAND is essential for end-use applications.

Characterization of 3D NAND
3D TLC, QLC, and Low Latency NAND

- 2D NAND limited to traditional SLC and MLC
- Early attempts at 2D TLC had limited utility
- Transition to 3D NAND enabled TLC & QLC

All three 3D NAND technologies present certain characterization challenges

- Competition with emerging memory technologies
- Precipitated low-latency NAND (3D SLC)
Transition to 3D NAND enabled TLC for mainstream applications

- Characterization of TLC depends on expected use-case
- 3D TLC has rapidly displaced 2D MLC
- Enterprise, consumer
- The more aggressive the application, the more demanding the characterization

Characterization of 3D TLC
3D TLC Displays High Endurance

- Lower BER after 21,000 P/E cycles
- Superior cycling endurance
- High quality of 3D TLC
- Transition to TLC presented challenges for characterization

While excellent for end-use case, while enabling wide adoption, 1st gen. 3D TLC showed lower BER after 21,000 P/E cycles.
TLC blocks have at least 3 different page types with different characteristics. Some manufacturers include MLC and SLC pages as well. Different page types respond differently to various NAND failure modes. Page quality can vary across block (3D cell stack). Understanding behavior of each page type requires full characterization. Worst-case page determines Bit Error Rate (BER) limits. TLC Page Bit Error Rate (BER) is divided into clear groups based on page type. At end of life, page Bit Error Rate limits are determined by the worst-case page.
Different TLC page types often have different read latency. MLC and SLC pages, if present, have different read latency as well.

Controller design must be robust against varying read latency. Should characterization focus on worse-case average read time or on worst-case read time or average read time? Depends on use-case.

Very wide variation (2-3x) in page read latency.

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**TLC NAND Cells Increasingly Crowded**

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- TLC NAND cells must support 8 independent cell states
- Cell distributions packed tightly – little margin for error
- As cells are subjected to cycling stress, problems arise
- Performance characterization required to understand impacts

For more information, see N. Papandreou et al., "Characterization and Analysis of Bit Errors in 3D TLC NAND Flash Memory," 2019 IEEE International Reliability Physics Symposium (IRPS), Monterey, CA, USA, 2019, pp. 1-6.

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**TLC Distribution @ Beginning of Life**

**Erase State Degradation**

**Widened Distributions**

**2-Step Programming Errors**

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**TLC Distribution @ End of Life**
Read Voltage Threshold Management

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8 independent cell states require 7 individual read thresholds to discriminate between.

Example TLC Cell Distribution

V<sub>TH</sub> 10 6 5 4 3 2 1 0

111 011 001 101 110 010 000

Trade-off between capability and complexity — characterization required.

Reactive recovery only? Proactive application of manufacturer read shift tools? Active tracking of all optimal read thresholds?

For more information, see N. Papandreou et al., "Characterization and Analysis of Bit Errors in 3D TLC NAND Flash Memory," 2019 IEEE International Reliability Physics Symposium (IRPS), Monterey, CA, USA, 2019, pp. 1-6.
Transition to 3D NAND has also enabled development of QLC NAND. Initial focus on read-intensive applications improved density and $/GB at cost of reduced endurance and timing parameters. Plus, some new complications.

3D QLC characterization has all the challenges of 3D TLC, only more so. Plus, some new complications.
3D QLC shows drastically reduced endurance relative to TLC. TLC cycling endurance is less important for read-intensive applications, but actually makes characterization faster!

Limited endurance of QLC places restrictions on end-use, but actually makes QLC BER after 1.5k cycles exceeds that of TLC after 12k cycles. Reduced endurance relative to 3D TLC shows singificantly Reduced Endurance.
QLC blocks have at least 4 different page types.

Some manufacturers include TLC and SLC pages as well.

At end of life, Page Bit Error Rate (BER) is divided into clear groups based on page type.

Page Bit Error Rate (Log)

Understanding behavior of each page type is particularly important for QLC – there is little margin for error, and every little bit helps.

3D QLC: Even More Page Types

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Average Read Latency for TLC is elevated over that of QLC

Wide Variation in QLC page-read latency

Variation

Read latency variation is even more pronounced than in TLC

Read latency is important design consideration for read-intensive applications

Controller design must be robust against read latency uncertainty
QLC has 16 states and 15 read thresholds

- Any approach requires extensive characterization and validation
- Management of read voltage thresholds more complex than in TLC
- Very little margin for error, especially after cycling wear

QLC Distribution at Beginning of Life
Low-Latency NAND being developed by some manufacturers to challenge emerging memory technologies. Designed to fit niche between traditional NAND and DRAM.

- Trade-off: reduced capacity and increased $/GB
- 3D TLC NAND read latency is ~75μs, DRAM is ~50ns
- 3D SLC NAND is 3D optimized for very low read latency (single-digit microseconds)
- Low-Latency NAND comes with its own characterization challenges.

Characterization of Low-Latency NAND

Single-Level Cell (SLC)
Low-Latency NAND supports fast reads.

- Low-Latency NAND is targeted at read-intensive applications where read latency is key.
- Data persistence provides additional advantage over traditional DRAM.
- Read latency must be extensively characterized.
- Characterization should ensure read latency can be guaranteed under all expected conditions.

Reads

Low-Latency NAND supports fast reads.
Low-Latency NAND shows extremely high endurance:
- Cycling endurance >50k cycles
- Extremely high endurance
- Very Low-Latency NAND shows high- 
  - Latency NAND
- BER far below end-of-life TLC/QLC BER even after 50k P/E cycles

High Endurance poses challenge for testing:
- If characterization cycling is too rapid, results not representative
- Characterization takes forever if characterization cycling is too rapid, results not representative
- Characterization can be accelerated using mixed-dwell time cycling

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The technology

Characterization must account for peculiarities of intended use-case

Characterization must be well-matched to each presents challenges for characterization

Each has unique product applications

3 Major Cell Types for 3D NAND

- Triple-Level Cell (3D TLC)
- Quadruple-Level Cell (3D QLC)
- Low-Latency NAND (3D SLC)

Overall Summary