Improving Quality of Service for 3D NAND SSDs Using LDPC Correction

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Problem Statement

- TLC and QLC 3D NAND technologies require LDPC correction just to withstand a few thousand program/erase cycles.
- LDPC gives its best correction performance through soft decoding, but that method requires read oversampling, that is, reading the same memory location multiple times.
- Besides the fact that this approach obviously reduces read bandwidth, it also lowers the Quality of Service (QoS) of SSDs, which is the key parameter in high-value data environments.
- Even short periods in which SSDs are non-responsive are generally unacceptable in such situations.
QoS

Read

IF FAIL

Read + Error Recovery Flow

Read Oversampling (i.e. multiple NAND Reads)
- Re-Read + HD
- Soft Reads + SD

QoS

HD=Hard Decoding
SD=Soft Decoding
QoS dependencies

SSD Controller
HW
FW

ECC

NAND

Error Recovery Flow

QoS
Fully Integrated SSD-NAND Characterization Flow

Latency, Bandwidth, IOPS

SSD Simulator

# channels
LDPC
WA
FTL
Flash IF
Workload
Host IF
NAND Characterization Setup

Real NAND Flash characterization with NVMe SSD controller:

• Endurance
• Retention (online/offline)
• RBER measurement
• Rack-scale testing
• TBs of data
LDPC Characterization Setup

FPGA implementation of Microchip ASIC Hard/Soft LDPC

- Real NAND Flash channel
- FER over BER computation
- Decoding performance calculation
- Rack-scale simulation
- Hundreds of billions of codewords per day
Full system level co-simulator for performance/QoS evaluation

SSD Simulator Architecture

Qemu

- USER APPLICATIONS
- WEB APPLICATIONS
- FILE SYSTEMS

Co-Simulation
Experimental Setup

• SSDExplorer is fed with data coming from characterization:
  • tRead, tProg, tErase, and RBER are measured from NAND
  • LDPC hard/soft decoding performance and FER are measured from a real LDPC implementation

• Simulated configuration:
  • 16 Channels
  • 8 die per channel
  • PCIe Gen3x4 (NVMe)
  • Real host workload (Qemu)
  • NAND Flash at End of Life
  • Error Recovery Flow: if Hard fails, then go to Soft (1 Bit)
Soft Read activation

• Soft Reads can be managed in 2 ways:
  • Soft Reads are initiated by the SSD Main Processor (FW management)
  • Soft Reads are initiated by the Flash Channel Processor (“local” management) -> in this case the SSD controller has to be properly designed
50%-50% 4kBytes Random Read/Write

![Chart showing comparison between SSD Main Processor and Flash Channel Processor QoS](chart.png)
100% 4kBytes Random Read
Conclusions

- TLC and QLC 3D NAND technologies require LDPC correction.
- LDPC gives its best correction performance through soft decoding, but that method requires read oversampling, thus impacting QoS.
- The impact of Soft Reads and Soft Decoding can be mitigated by a specific design of the SSD Controller.
- We have proven that QoS can significantly be improved if Soft Reads can be initiated by the Flash Channel Processor inside the SSD Controller.
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