MRAM Developers Day
August 2019

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# Agenda

1. GF View of Market Dynamics and Strategy
2. MRAM on 22FDX®
3. MRAM on 12LP+
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1. GF View of Market Dynamics and Strategy
2. MRAM on 22FDX®
3. MRAM on 12LP+
Market Consensus: Memory challenges by Node

- Data/Code Storage: eFLASH
- Working Memory: SRAM

Most pressing issue facing industry: Adv. Node Auto-G1 Solution need

Devices:
- eMRAM-F
- eMRAM-S
- ePClM (<28nm ?)

Node Sizes:
- 90nm
- 55/40nm
- 32/28nm
- 22nm
- 14/12nm
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MRAM Meets Growth Driver’s Needs: High Density, Low Power Memory with 22FDX® Platform

SOI + RF + MRAM a powerful platform

• SOI ← Back Bias power optimization
• RF ← SOI efficiency
• MRAM ← persistence for power cycling

Differentiated and optimized for ‘connected MCU based applications and emerging AI edge and AR

Leading clients applications:
BTLE, IoT Wearables, Edge AI, Low power consumer, Low power ISM, Next generation GenPur MCUs
Memory challenges by Node. General consensus in market.

Data/Code Storage

eFLASH

Most pressing issue facing industry

eMRAM-F
ereRRAM
erePCM (<28nm ?)
eFLASH replacement needed 28nm node and beyond….  

…GF’s Key assertions on the 2x eNVM node:

28nm designs will stay with low-risk ESF3 eFLASH solution

- 28nm MRAM and PCM may struggle to get traction (too risky)
- 28nm PCM has burden of poor <28nm foundry roadmap

22nm MRAM-F from GF was architected to be as Flash like as possible

- Other 2x node MRAM solutions are more ‘SRAM like’ and less ‘Flash like’
- 22FDX MRAM is robust (5x solder reflow) and has 2yr road-map to Auto-G1
- How about RRAM for eFLASH replacement at the 2x Node?
  • Demonstrated 125C support? Auto-G1 roadmap?
Value Proposition 22FDX® eMRAM-F: Like eFLASH – only better!

Next Best Alternative Analysis (Vs 28nm eFLASH):
- 3+1 MRAM masks Vs 11+ for eFLASH – lower cost
- Better write speed
- Better endurance
- Better write power
- Better data retention ( 
- Roadmap to 1x nodes
- Paired with 22FDX SOI platform

<table>
<thead>
<tr>
<th>Spec</th>
<th>22FDX MRAM-F</th>
<th>eFlash</th>
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<tbody>
<tr>
<td>Leakage</td>
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<tr>
<td>Density</td>
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<td>Read Power</td>
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<td>Adv Node Roadmap</td>
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<td>Mask Layers</td>
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<td>22FDX Platform</td>
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<tr>
<td>Write Speed</td>
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<td>Macro Support</td>
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<td>Ext. temp support *</td>
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<td>Maturity</td>
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* Auto Grade 1 MRAM target 1H 2021
Moves MRAM score to a 4
Yield and Endurance
Yield Data

40Mb eMRAM $t_0$ BER ($< 6E-6$) yield improvement trend over time.

Achieved 100% yield at 6E-6 BER on some wafers.
Average *Intrinsic Yield* in low 90’s *without* ECC and Redundancy
Cycling endurance data of 40Mb eMRAM package parts at -40, 25 and 125°C after every interval of cycles up to 1M cycles.

All the parts passed endurance failure rate criteria of 1 ppm.

Bit-cell resistance distributions of $R_p$ and $R_{ap}$ states from 128Kb cell array before and after 1M endurance cycling.

No degradation in resistance observed after 1M endurance cycling.

Projected number of cycles from TDDB (time dependent dielectric breakdown) data versus voltage at 25 °C for failure rate of 1 ppm.

Macro has margin to endurance requirement of $>1E6$ cycles at $V_{op}$. 
Magnetic Immunity
MRAM Magnetic Immunity

eMRAM

eMRAM designers need to consider exposure to strong (DC) magnetic fields for data retention. (minimal temp and endurance effects)

MRAM writing (and reading) in the presence of a strong magnet field needs to be considered

eFlash

eFLASH designers need to consider endurance and temperature effects on data retention.

Active eFLASH write and read disturb need to be considered
Stand-by magnetic immunity at 25, 55 and 105 °C for 20 min magnetic field exposure.

10 years projection shows 0.1 ppm failure rate below ~600 Oe at 105 °C.

Read disturbance shmoo data with magnetic field sweep at 25 and 125 °C

No read disturb up to 900 Oe at 125 °C

No significant endurance induced changes in magnetic immunity observed
Writing MRAM in a Magnetic Field

WER (write error rate) plots of 40Mb eMRAM macro under zero, +/- 500 Oe field at 25 °C

GF 22FDX MRAM can be written in +/- 500 Oe magnetic field with no significant degradation to write error rate (WER)

Cycling endurance data at -40 °C under zero and +/-500 Oe magnetic field to cover active mode magnetic immunity

No measurable effect on 1M cycle endurance failure rate during write in presence of +/- 500 Oe magnetic field
Magnetic Field Industry Spec.

- <100 Oe is enough for most of normal uses

**Biological Effects**
- Impairment of heart function
- Malfunction in central nervous system
- Possible changes in protein and DNA
- Minor biological influences
- No effect

**Magnetic Field (Oe)**

<table>
<thead>
<tr>
<th>Earth (static)</th>
<th>ICNIRP*</th>
<th>IEC-61000-4-8**</th>
<th>surface of speaker</th>
<th>HDD magnet</th>
<th>Magnetic Card</th>
<th>MRI/Degausse</th>
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<tr>
<td>0.5</td>
<td>&lt;4.5</td>
<td>&lt;12.6</td>
<td>~60</td>
<td>&gt;2000</td>
<td>&gt;4000</td>
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<tr>
<td></td>
<td>for worker</td>
<td>for public</td>
<td></td>
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</table>

10Yr 105C 580Oe projection

- Most applications <100 Oe
- Intentional use >5000
- Accidental use

### Notes:

- * The International Commission on Non-Ionizing Radiation Protection (ICNIRP)
- ** European Union, IEC-61000-4-8, on the magnitude of magnetic fields that a device can experience under normal operation. The maximum value of 12.6 gauss
- Oe → Oersted is \(1000/4\pi \approx 79.5774715\) amperes per meter. i.e. The H-field strength inside a long solenoid wound with 79.58 turns per meter of a wire carrying 1 A is approximately 1 oersted.
Solder Reflow
Solder Reflow

260C x 1 min x 5 → 5x Reflow

Post 5x refloors BER improvement trend for different MTJ processes.

Inset shows 100% 5x reflow performance across wafer for 10 ppm BER criteria

Post 5x reflow BER of 40Mb eMRAM package parts for $R_p$ and $R_{ap}$ states.

All the parts passed 1 ppm criteria after 5x reflow.
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Disruptive MRAM-S at the 1x node

**Disruptive technology value...**

- Clients seek *PPA reward for technology & architectural risk*
- Seeking >2x over incumbent tech in PPA (Pwr/perform/Area) metric
- Advance node eNVM bit cell size *limited* by drive transistor

**MRAM-S as SRAM replacement compelling on 12LP+**

- 2x node MRAM-S >1/2 area SRAM-HD. Risk/Reward unfavorable
- 12LP+ MRAM-S <1/2 area SRAM-HD. Risk Reward favorable
- Power (Persistence & Area drive MRAM-S on 12LP+.
  - Lwr Pwr./Heat as disruptive SRAM replacement technology
  - Emerging use of MRAM-S for stochastic computing in AI/ML (?)