Flash Memory Summit

Using MRAM to Enable Power Loss Protection of Data for NVMe

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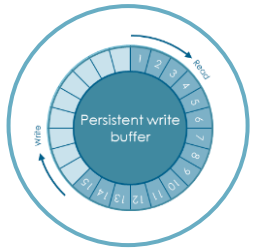
Why STT-MRAM is a great choice?

- **Persistence –** STT-MRAM is inherently a non-volatile memory technology. No batteries or bulk caps needed
- **Density -** 1Gb density provides bigger persistent buffer sizes for most applications in limited board space
- **Throughput performance R/W –** DDR4 w/ x16 interface provides throughput of 2.7GBps with single device
- **Data endurance –** Endurance in excess of 10's of billions of cycles does not require any wear-leveling for NVMe block workloads
- **Latency response time / QoS (ns) –** Design built with STT-MRAM provides ultra low and deterministic latencies with virtually no tail
- **Data retention time (Years) –** Provides data retention for up to 10+ years at 85C
- **Bit error rate (BER) –** Enable enterprise class designs with off the shelf SEC-DED ECC schemes
- **Product reliability –** Develop highly reliable and top quality products without worrying about operating temperature range, capacitor and battery problems

STT-MRAM: Use cases for NVMe designs?

Power loss protected
Write Buffer

Power loss protected
Scramming Memory



Power loss protected
Ring Buffers

Power loss protected
Journaling

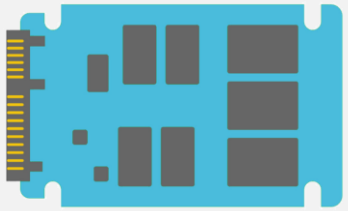
High Performance
Logging

Application Requirements

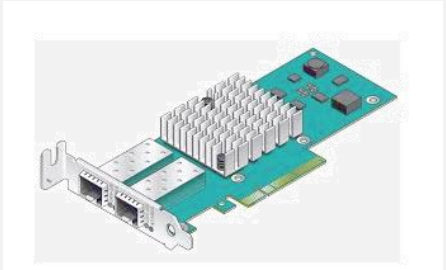
Write Performance	QoS (Low Latency)	Reliability	Persistence	Endurance

STT-MRAM: Target NVMe Applications

1 **PCIe SSDs (NVMe)**
For PLP Buffer



2 **Fabric Accelerators**
For NVMe-oF & NVMe/TCP



3 **Storage Accelerators**
For AFA & Hybrid Arrays

PLP Write Buffer for NVMe SSD

128MB+ large Buffer For *Low Latency*	10X More Space For *Streams and ZNS zones*	Simplified Architecture Speeds *Time To Market*	More Space For NAND *Memory*	Improved System *Reliability*	Support *PMR*
High QOS	*Extended Drive Life*	*Increased Value Capture*	*Higher Storage Density*	*Lower Failure Rates*	*Enable PMR on space constrain FF*

STT-MRAM can make your QLC based NVMe designs faster, better, more reliable and durable

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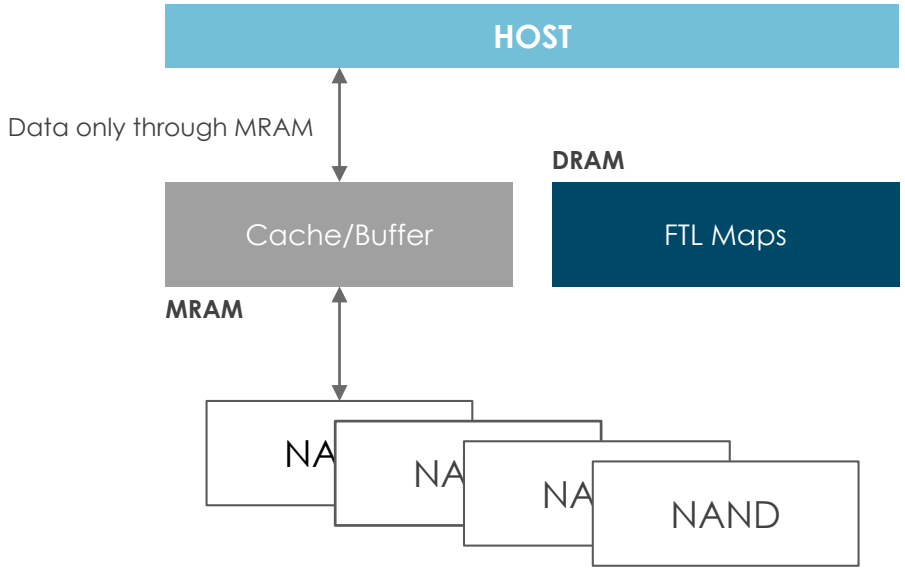
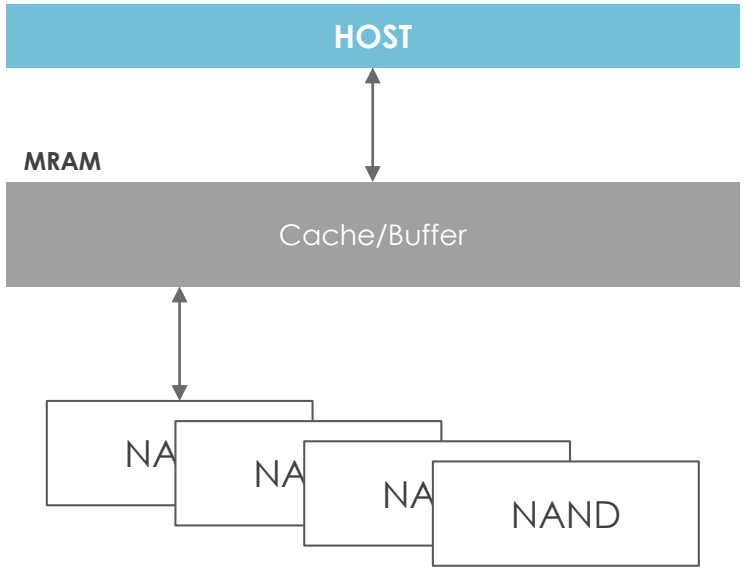
NVMe SSD Implementations

TRADITIONAL ENTERPRISE SSD



- MRAM as buffer/cache
  - Data in flight
  - Delta FTL
- FTL in DRAM
- Caps are eliminated
- Additional MRAM power

OPEN CHANNEL/ZNS SSD



- MRAM replaces DRAM completely
  - Data in flight
  - Zones metadata
- FTL in host DRAM
- Lower BOM cost
- Caps are eliminated

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Fabric Accelerator Purpose
Higher Performance & Agility

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- **Provide sub-µSec latency from wire to application data persistence**
  - Kernel bypass
  - Host CPU bypass
  - Host memory bypass
  - Peer-to-Peer data transfers
  - RDMA termination
- **Offload CPU computation cycles**
- **Customer configurable offload engines**
  - ARM CPU code or FPGA code
- **Provide higher write/read data throughput**
- **Enable simpler, lower power and lower cost appliance designs**
  - Without need for x86 Server CPUs i.e. target ARM

Data flow for NVMe-oF or NVMe/TCP

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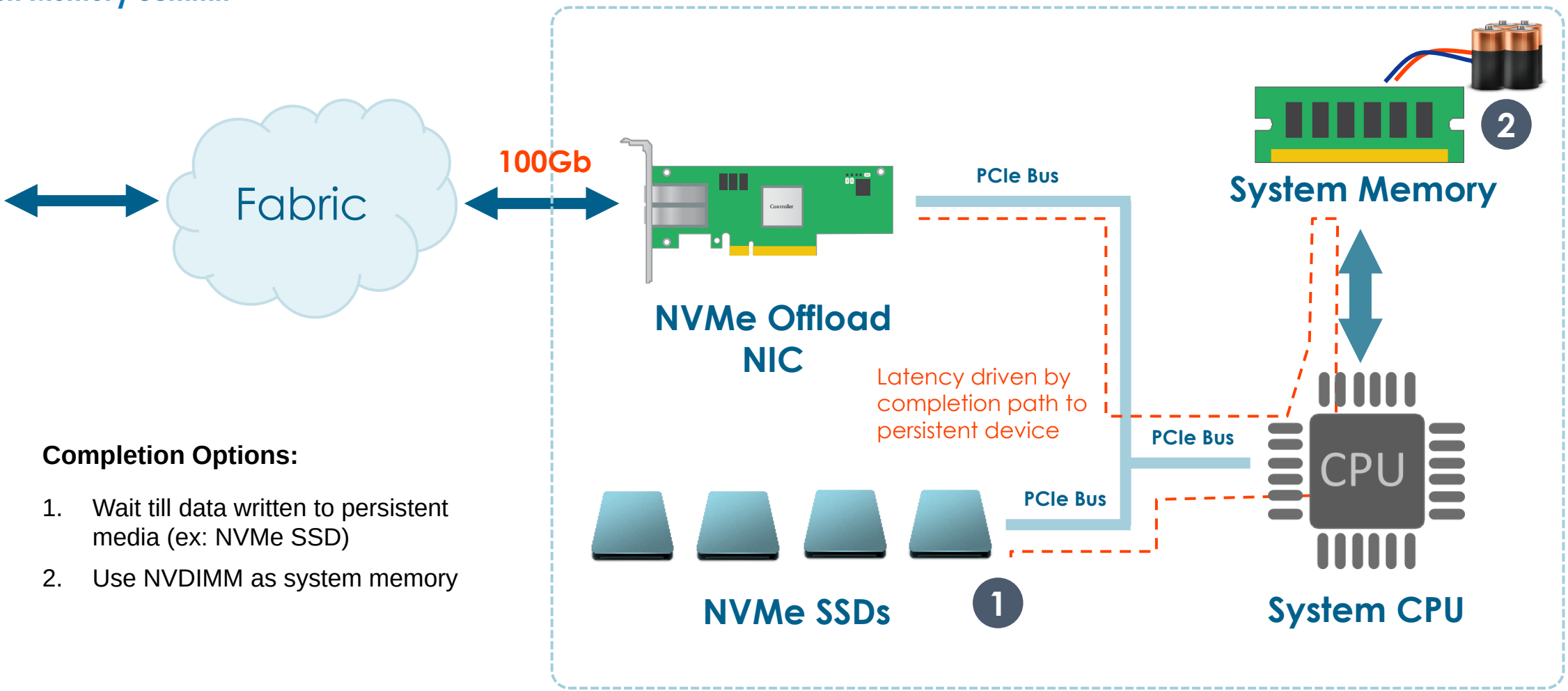

Completion Options:

1. Wait till data written to persistent media (ex: NVMe SSD)
2. Use NVDIMM as system memory

STT-MRAM Value Proposition

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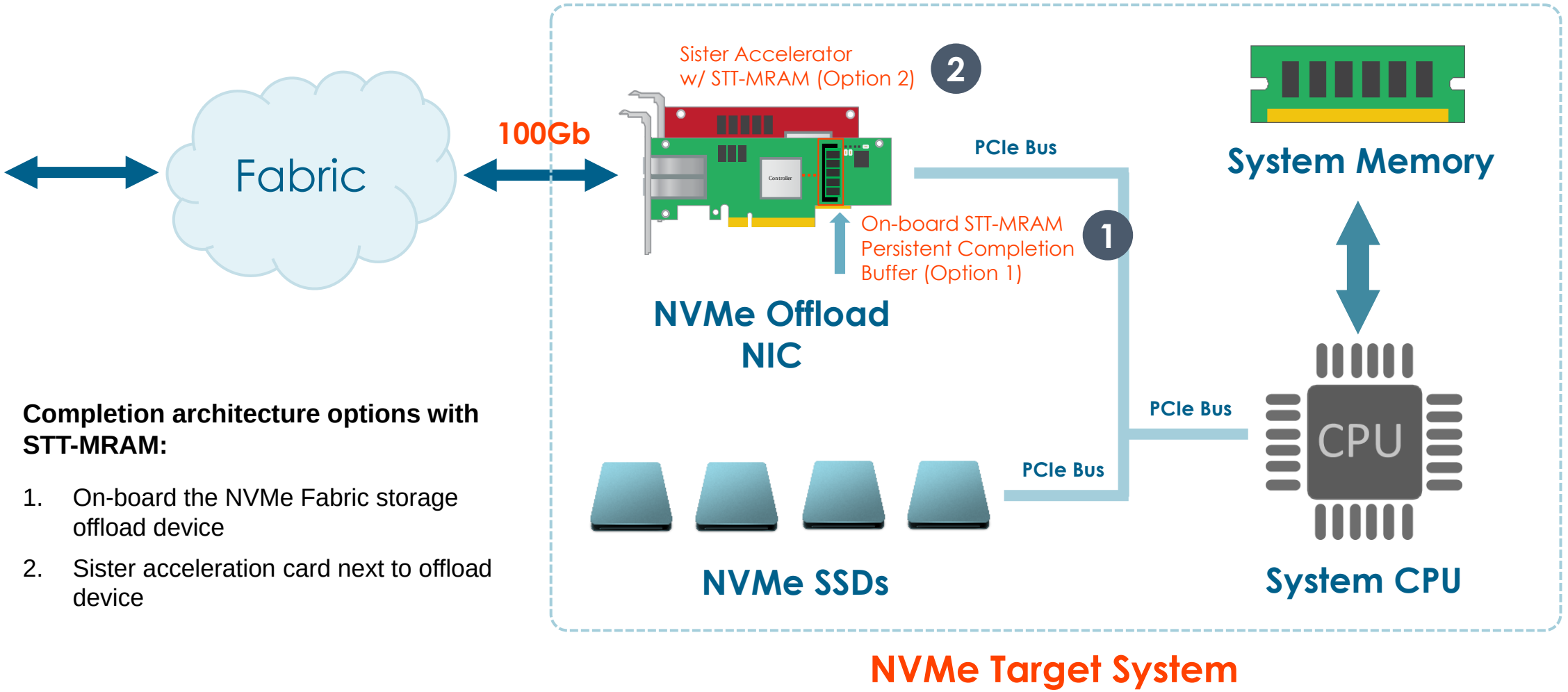

Completion architecture options with STT-MRAM:

1. On-board the NVMe Fabric storage offload device
2. Sister acceleration card next to offload device

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Storage Accelerators for All Flash Arrays

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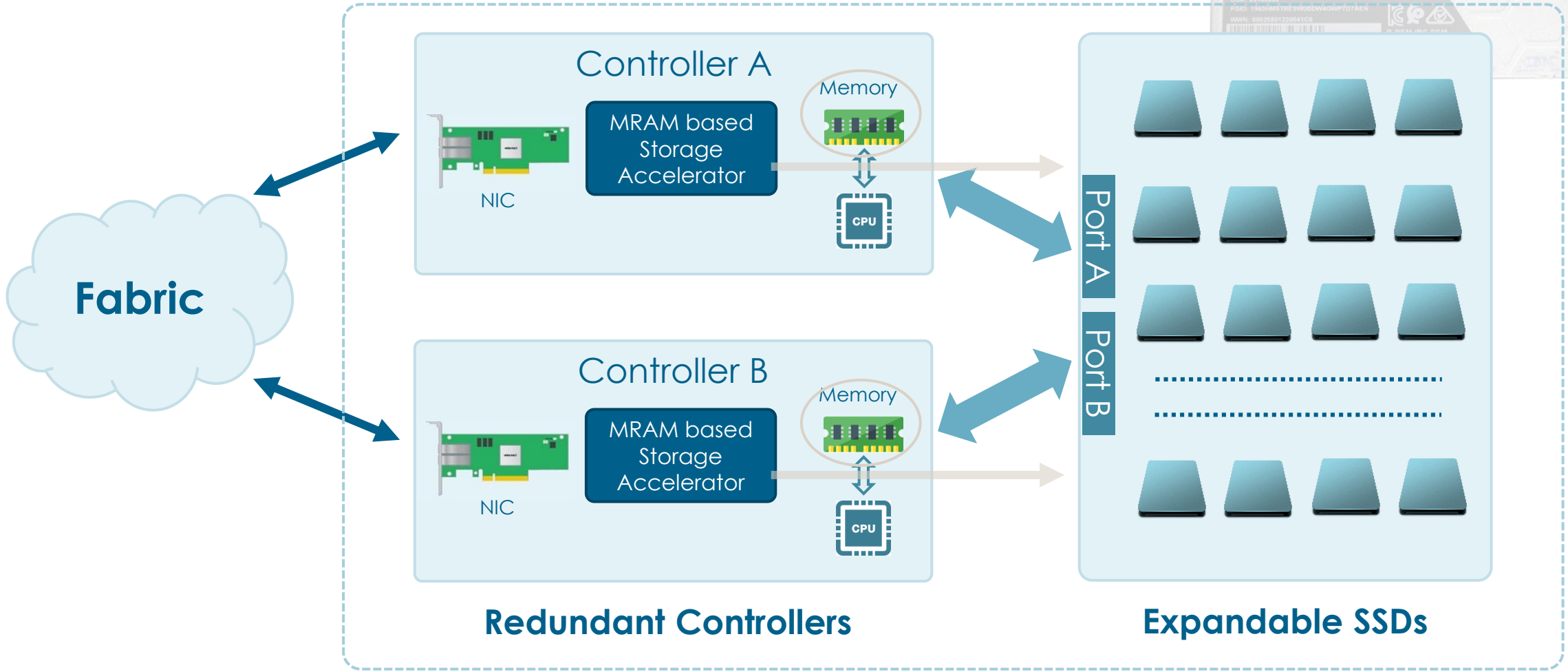

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Why MRAM for Storage Accelerators

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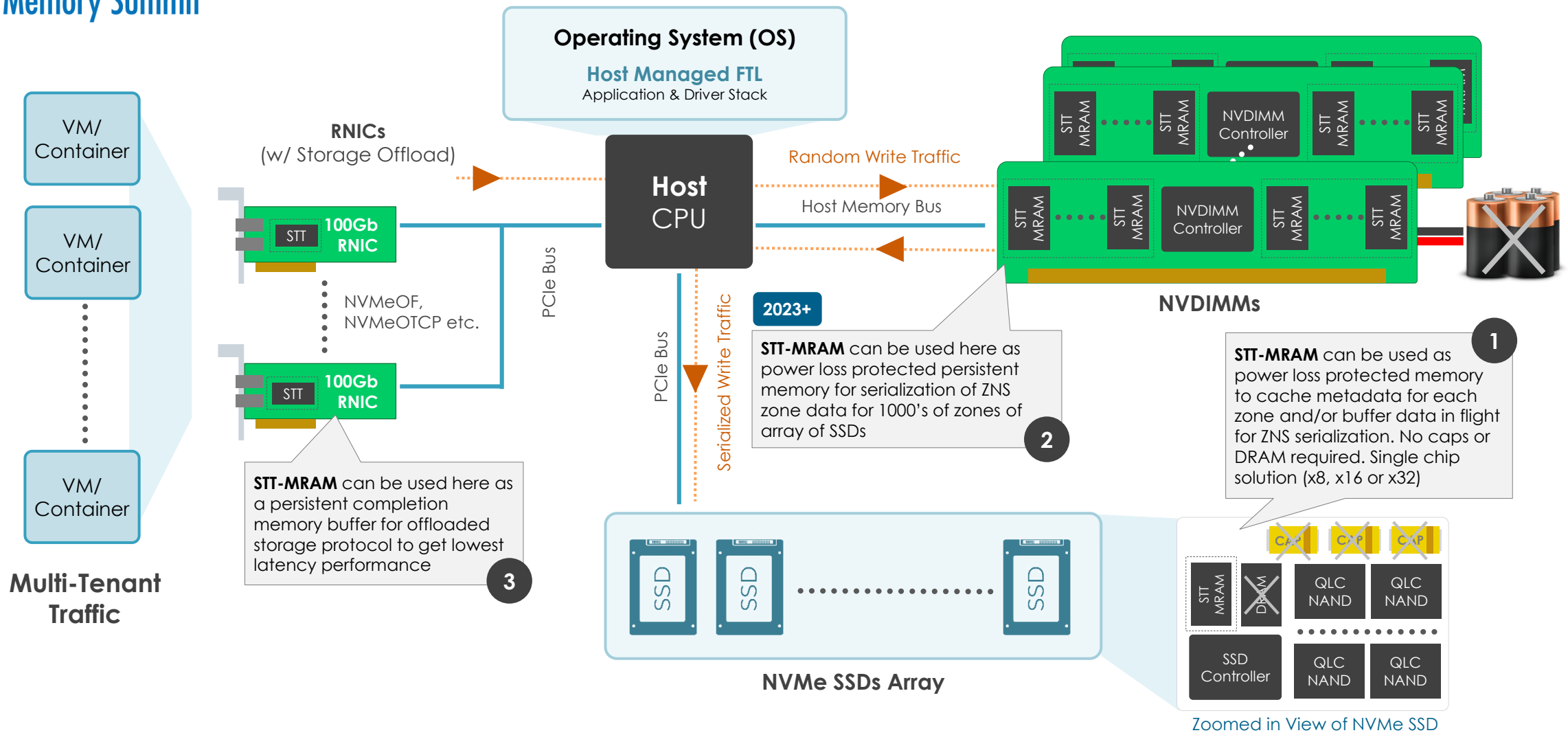
- Better Reliability
- Better IOPs and Latency performance
- Thermal Performance
- Better long term TCO
- Better U.2 form-factor product
- No waiting for battery or supercaps recharge on boot
- No serviceability of battery or supercaps required

Wrap-up: STT-MRAM in a NVMe Ecosystem



Design your next NVMe product with STT-MRAM

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Buy MRAM enabled DDR IP from
Synopsys or Cadence

SYNOPSYS®

Design VIP:

David Pena

djap@cadence.com

cadence®

Design IP:

Mark Greenburg

mgreenberg@cadence.com

Use standard SEC ECC to achieve 1E-20 UBER

Dedicated ECC: **No change required**

Inline ECC: **Supported**

Minimal FW changes required for MRAM support and it will eliminate complex PLP design

DDR IP **incorporates power on/off sequences** required for persistence

3 SSD controller companies planning to support STT-MRAM

MRAM based SSDs will be **shipping in 2020**

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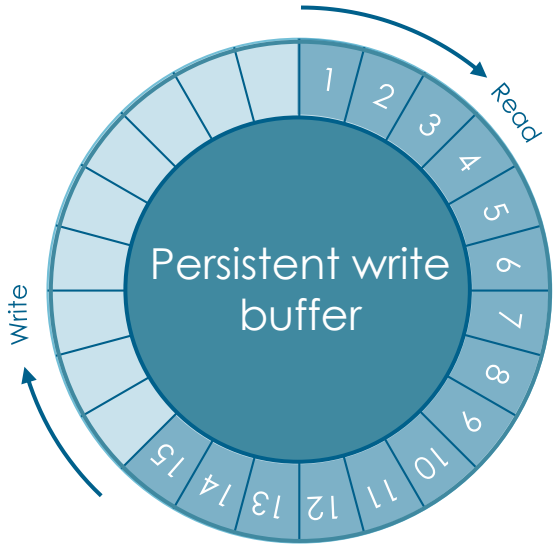
Backup

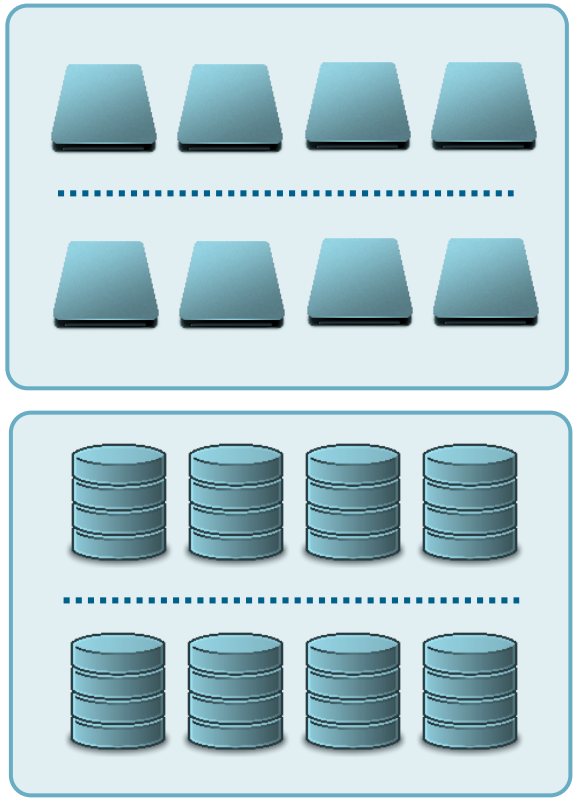
STT-MRAM: Low Latency Write Burst Buffer

Get Higher Overall System Application Performance By Using STT-MRAM As Write Buffer

Incoming Data

- Variable Rate
- Bursts
- Latency sensitive





Application Requirements

Power Loss Protection
Persistent Data
Low Latency & High Performance

Written to in big block sizes