Memory Class Storage

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Where is DRAM Headed?

DRAM density used to double every 3 years

Now doubling takes 6 years

...but DDR5 ends at 32Gb...
DDR5 Ends at 32Gb?? Really??

But the DDR5 data sheet shows a 64Gb chip!

However, to get 64Gb, you have to give up 3DS…

<table>
<thead>
<tr>
<th>Function</th>
<th>Abbreviation</th>
<th>CS</th>
<th>CA PINS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Activate</td>
<td>ACT</td>
<td>L R0 R1 R2 R3</td>
<td>B0 B1 B2 B3</td>
</tr>
<tr>
<td></td>
<td></td>
<td>H R4 R5 R6 R7 R8 R9</td>
<td>R0 R1 R2 R3</td>
</tr>
<tr>
<td>Write</td>
<td>WR</td>
<td>L H H H BL*</td>
<td>A0 A1 A2 A3</td>
</tr>
<tr>
<td></td>
<td></td>
<td>C3 C4 C5 C6</td>
<td>C7 C8 C9 C10</td>
</tr>
<tr>
<td>Read</td>
<td>RD</td>
<td>L H H H BL*</td>
<td>A0 A1 A2 A3</td>
</tr>
<tr>
<td></td>
<td></td>
<td>C2 C3 C4 C5</td>
<td>C6 C7 C8 C9</td>
</tr>
</tbody>
</table>
Chip IDs (CIDs) select a DRAM within a stack

Up to 16 32Gb DRAMs may be stacked

Only 8 64Gb DRAMs may be stacked

16 x 32 = 8 x 64 = 512Gb per 3DS stack maximum
The Universe of Storage Class Memories (Persistent Memories)

Many technologies coming online to fill the gap between DRAM and Flash.
## Overview: Storage Class Memories

<table>
<thead>
<tr>
<th>Memory Type</th>
<th>Non-volatility</th>
<th>Endurance</th>
<th>Read Time (ns)</th>
<th>Write Time (ns)</th>
</tr>
</thead>
<tbody>
<tr>
<td>DRAM</td>
<td>No</td>
<td>10^{15}</td>
<td>10</td>
<td>10</td>
</tr>
<tr>
<td>MRAM</td>
<td>Yes</td>
<td>10^9</td>
<td>50</td>
<td>100</td>
</tr>
<tr>
<td>ReRAM</td>
<td>Yes</td>
<td>10^6</td>
<td>200</td>
<td>1000</td>
</tr>
<tr>
<td>PCM / 3DXpoint</td>
<td>Yes</td>
<td>10^6</td>
<td>100</td>
<td>1000</td>
</tr>
<tr>
<td>FeRAM</td>
<td>Yes</td>
<td>10^{14}</td>
<td>50</td>
<td>50</td>
</tr>
<tr>
<td>Flash</td>
<td>Yes</td>
<td>10^3</td>
<td>50M</td>
<td>25M</td>
</tr>
</tbody>
</table>

### Chasm

Changing “SCM” to “Persistent Memory” doesn’t help... In fact, it may make it less clear...
The NVDIMM-P Protocol

NVDIMM-P protocol invented to handle memory with low endurance

Non-deterministic credit based system allows time for “clean-up”

Out-of-order data returned with ID
Carbon nanotubes connected or split using electrostatic force

Stochastic array of tubes forms a resistive matrix

Stackable into a crosspoint memory array

For details, attend my talk at Hot Chips, September 2018
Unlimited Write Endurance

NRAM carbon nanotube bonds are atomic
Once made, they stay connected until disrupted
Insensitive to heat, radiation, etc.
No CNT failure has been detected
Unlimited write endurance expected
What can you do with a 10 ns core speed?

Not only perform as a DDR4 SDRAM

With non-volatility

And add the ECC on-the-fly function of DDR4E
RDIMM = NVDIMM

With inherent non-volatility, an RDIMM is an NVDIMM

No need for backup & restore procedure nor for battery backup
Introducing Memory Class Storage

Industry primed for a DRAM replacement technology

- Hard Disk
- SSD
- NVMe
- Wasteland
- DDR DRAM
- Flash
- Phase Change
- 3D Xpoint
- Resistive RAM
- Magnetic RAM
- DDR NRAM

> DRAM performance
= DRAM endurance
> DRAM capacity
< DRAM price
## Memory Class Storage vs SCM

<table>
<thead>
<tr>
<th></th>
<th>DRAM</th>
<th>NRAM</th>
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<tr>
<td>Non-volatility</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>Read Time</td>
<td>10 ns</td>
<td>10 ns</td>
</tr>
<tr>
<td>Write Time</td>
<td>10 ns</td>
<td>10 ns</td>
</tr>
<tr>
<td>Endurance</td>
<td>$10^{15}$</td>
<td>$10^{15}$</td>
</tr>
<tr>
<td>Read Time</td>
<td>10 ns</td>
<td>10 ns</td>
</tr>
<tr>
<td>Write Time</td>
<td>10 ns</td>
<td>10 ns</td>
</tr>
</tbody>
</table>

### Storage Class Memory

<table>
<thead>
<tr>
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<th>MRAM</th>
<th>ReRAM</th>
<th>PCM / 3DXpoint</th>
<th>FeRAM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Non-volatility</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Read Time</td>
<td>$10^9$</td>
<td>$10^6$</td>
<td>$10^6$</td>
<td>$10^{14}$</td>
</tr>
<tr>
<td>Write Time</td>
<td>50 ns</td>
<td>200 ns</td>
<td>100 ns</td>
<td>50 ns</td>
</tr>
<tr>
<td>Endurance</td>
<td>$10^{15}$</td>
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<tr>
<td>Write Time</td>
<td>1000 ns</td>
<td>1000 ns</td>
<td>1000 ns</td>
<td>50 ns</td>
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</table>

### Storage

- Flash
  - Non-volatility: Yes
  - Read Time: $10^3$ ns
  - Write Time: 50M ns
  - Endurance: 25M ns

...aka “Persistent Memory”
When DRAM Ends…

**DRAM**

End of the line
32Gb mono
512Gb 3DS

- 8Gb → 16Gb
- DDR4 → 5
- 3DS 8H → 16H
- 16Gb → 32Gb

Santa Clara, CA
August 2018
...NRAM just begins...

**DRAM**

- End of the line
- 32Gb mono
- 512Gb 3DS

**NRAM**

- More layers CNT
  - 512Gb

- Roadmap continues
  - 512Gb mono
  - 8Tb 3DS

- New process
  - 256Gb

- DDR4 → 5
  - 3DS 8H → 16H

- New process
  - 16Gb
  - 32Gb
  - 64Gb
Density Roadmap

- 4 layers of CNT
  - 16Gb @ 28 nm
  - 64Gb @ 14 nm
  - 256Gb @ 7 nm

- 8 layers of CNT
  - 32Gb @ 28 nm
  - 128Gb @ 14 nm
  - 512Gb @ 7 nm

- 16Gb per layer
  - 14 nm

- 64Gb per layer
  - 7 nm

- 4Gb per layer
  - 28 nm
### Existing

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<td>ACT</td>
<td>L</td>
<td>CA0 CA1 CA2 CA3 CA4 CA5 CA6 CA7 CA8 CA9 CA10 CA11 CA12 CA13</td>
</tr>
<tr>
<td></td>
<td></td>
<td>H</td>
<td>R0 R1 R2 R3 BA0 BA1 BG0 BG1 BG2 CID0 CID1 CID2/ DDPI0</td>
</tr>
</tbody>
</table>

### Row Extension

- **REXT A**: ACT
- **REXT B**: ACT
- **REXT C**: ACT
- **REXT A**: ACT

### New Command

- **A+ROW**: REXT A
- **A+ROW**: ACT
- **A+ROW**: ACT
- **B+ROW**: ACT
- **B+ROW**: ACT
- **C+ROW**: ACT
- **A+ROW**: ACT

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**Proposal before the JEDEC Committee**
### Extended Addressing Protocol

**64 Gb Addressing Table, Option 2**

<table>
<thead>
<tr>
<th>Configuration</th>
<th>16 Gb x4</th>
<th>8 Gb x8</th>
<th>4 Gb x16</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bank Address</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bank Group Address</td>
<td>BG0*BG2</td>
<td>BG0*BG2</td>
<td>BG0*BG1</td>
</tr>
<tr>
<td>Bank Address in a BG</td>
<td>BA0*BA1</td>
<td>BA0*BA1</td>
<td>BA0*BA1</td>
</tr>
<tr>
<td># BG / # Banks per BG / # Banks</td>
<td>8 / 4 / 32</td>
<td>8 / 4 / 32</td>
<td>4 / 4 / 16</td>
</tr>
<tr>
<td>Extended Row Address</td>
<td>R17</td>
<td>R17</td>
<td>R17</td>
</tr>
<tr>
<td>Row Address</td>
<td>R0*R16</td>
<td>R0*R16</td>
<td>R0*R16</td>
</tr>
<tr>
<td>Column Address</td>
<td>C0*C10</td>
<td>C0*C9</td>
<td>C0*C9</td>
</tr>
<tr>
<td>Page Size</td>
<td>1 KB</td>
<td>1 KB</td>
<td>2 KB</td>
</tr>
</tbody>
</table>

**Chip IDs / Maximum 3DS Stack Height**
- CID3^0 / 16H
- CID3^0 / 16H
- CID3^0 / 16H

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**1 Tb Addressing Table**

<table>
<thead>
<tr>
<th>Configuration</th>
<th>256 Gb x4</th>
<th>128 Gb x8</th>
<th>64 Gb x16</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bank Address</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bank Group Address</td>
<td>BG0*BG2</td>
<td>BG0*BG2</td>
<td>BG0*BG1</td>
</tr>
<tr>
<td>Bank Address in a BG</td>
<td>BA0*BA1</td>
<td>BA0*BA1</td>
<td>BA0*BA1</td>
</tr>
<tr>
<td># BG / # Banks per BG / # Banks</td>
<td>8 / 4 / 32</td>
<td>8 / 4 / 32</td>
<td>4 / 4 / 16</td>
</tr>
<tr>
<td>Extended Row Address</td>
<td>R17*R21</td>
<td>R17*R21</td>
<td>R17*R21</td>
</tr>
<tr>
<td>Row Address</td>
<td>R0*R16</td>
<td>R0*R16</td>
<td>R0*R16</td>
</tr>
<tr>
<td>Column Address</td>
<td>C0*C10</td>
<td>C0*C9</td>
<td>C0*C9</td>
</tr>
<tr>
<td>Page Size</td>
<td>1 KB</td>
<td>1 KB</td>
<td>2 KB</td>
</tr>
</tbody>
</table>

**Chip IDs / Maximum 3DS Stack Height**
- CID3^0 / 16H
- CID3^0 / 16H
- CID3^0 / 16H

Extends addressing to 4Tb (512 GB) per die or 64Tb (8 TB) per 3DS stack
The Post-DRAM Age is Inevitable

Deep Learning

Artificial Intelligence

Self Driving

Data Mining

In-memory Computing

Memory demand is only headed north
What are you going to do after 32Gb?
Summary

DRAM is going away after 32Gb

“Storage Class Memory” fills a gap between DRAM and Flash

NVDIMM-P protocol allows SCM to share a DRAM channel

NRAM defines a new “Memory Class Storage” category

MCS = Unlimited write endurance and full DRAM speed

NRAM process roadmap extends beyond DRAM by > 16X
Questions?

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