Self-Adaptive NAND Flash DSP

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Outline

- NAND Flash Data Error Recovery
- Challenges of NAND Flash Data Integrity
- A Self-Adaptive DSP Technology to Improve NAND Flash Memory Data Integrity
NAND Trends

- Smaller feature size and more 3-D layers
  - Larger Vth variance

- More bits per cell
  - Less Vth margin
Advanced ECC technologies are applied in flash controller to compensate the increasing error bits in NAND flash memory.

Due to the soft decoding, the error correction performance of LDPC is significantly better than BCH.
Data Error Recovery

- On-the-fly LDPC Hard Decoding
- LDPC HD Retry
- LDPC Soft Decoding
- RAID

- Better Error Recovery
- Less Error Recovery Latency
Non-optimum read voltage dramatically increases BER from NAND.

Non-optimized soft data read degrades the LDPC soft decoding margin.
NAND Flash Data Integrity Challenges

- Process variance
  - New layer disparity in 3D NAND
- Program/erase cycling
- Data retention time
- Read Disturb
- Program Disturb
- Wide operation temperature range
- Other unexpected events
- ...

3D TLC NAND A

3D TLC NAND B
NAND Read Voltage Calibration

- NAND read reference voltage calibration significantly improve data integrity
  - Less bit errors for hard decoding
  - More accurate reliability information for soft decoding
Real World is Tough

- NAND voltage distribution is the function of too many factors
  - Some factors are impossible to be tracked
  - Retrying all cases leads to long read latency
Self-Adaptive NAND DSP

- Speed up data error recovery for both LDPC hard decoding and soft decoding
  - Collect more information about the read data block
  - Learn from previous failed LDPC decoding
  - Utilize time and spatial locality to learn from other NAND read data block
Big Data of NAND Analysis

- PE cycle & Retention

- Read disturb

- Physical Location
Some factors that impact VREF are difficult to track, such as temperature history...

However, due to the time and spatial locality of the NAND flash access, we can optimize NAND read reference voltage by learning from history.

NAND blocks in a super block are at the similar condition due to the parallelism scheme of NAND write.

The data in the same super block are very likely to be read in a short time interval.
Self-Adaptive NAND VREF Tracking Flow

1. Learn from offline big data
   - FW NAND Info.
     - PE/WL/Read #/ …
   - VREF Table

2. Learn from read history
   - Adjacent Retry Log
     - Block Retry Log

3. Self learning from LDPC decoding, such as error count/syndrome
Despite the impressive growth of bit density, NAND flash memories increasingly subject to worse raw storage reliability.

Affected by too many process and usage factors, NAND flash characterization of the threshold voltage distribution varies in its lifetime, which makes it a challenging issue to NAND flash controller.

Maxio’s self-adaptive NAND DSP technology is proposed to dynamically track NAND characterization.

Besides the static NAND characterization, this DSP technology on-the-fly learns NAND voltage distribution from previous NAND reads and dynamically adjusts the NAND read voltage.

Combined with strong LDPC codes, Maxio’s self-adaptive NAND DSP technology can significantly improve data reliability, extend NAND lifetime and shorten read response latency.
Thank you!