The programmable Flash emulation system

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The programmable Flash emulation system

- The Architecture of a typical SSD Controller
- The design target of Flash Controller
- Traditional verification method for Flash Controller
- The programmable Flash emulation system
- The BIT flip generator based on deep learning algorithm
Architecture of SSD Controller

- Host
- Front-end interface controller
  - RAM
  - CPU
  - DMA
  - Sensor
  - HW accelerator
- Backend flash controller
  - NAND
  - NAND
  - NAND
- SATA
- PCIe
- ONFL
- Toggle
- NAND
- NAND
- NAND
The design target of Flash Controller

- Interface compatibility
- Exception handling capability
- Parallel processing capability
- Extension ability
- Error correction ability
- Hardware and software co-design
Traditional verification method of Flash controller

Software simulation platform
- Test case
- Design files for Flash controller
- Different NAND Flash model files

Hardware verification platform
- Test case
- DVT Firmware
- Flash controller
- Different NAND chip

Software simulation verification
FPGA verification
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Host control center

Input test case

Return test result

Input configuration information

Test framework

Flash driver

Flash controller

ONFI

Toggle

Flash emulator

FPAG verification platform
Host control center

- Interface management
- Test platform management
- Configuration management
- Test case management
- Monitor test status
- Save test result
- Generate test report

Data base

FPGA Test platform
Flash emulator

FPGA Test platform
Flash emulator

FPGA Test platform
Flash emulator
FPGA verification platform

Test framework
- Receive test case
- Parse test case
- Organize flash command
- Send flash command
- Monitor flash status
- Handle command result
- driver

Host control center

Flash controller

Flash chip or Flash emulator
Flash emulator

Host control center

Flash interface simulation

Flash memory controller

Flash emulator

Electrical characteristics simulation

- Handle configuration
- Parse flash command
- Parse flash address
- Execute command
- Control flash status
- BIT flip generator
The programmable simulation system

Host control center

Test case input

Configuration input

Test result processing
Test case management
Configuration information management

Flash command parsing
Execute Flash command
Flash status control
BIT flip generator

Receive test cases
Parsing test cases
Send Flash CMD
Monitoring flash state
Processing command results

ONFI

Toggle

FPGA Test platform

Flash emulator

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The BIT flip generator based on Deep learning algorithm

- Data collection
- Build model
- Training and learning
- Adjust parameters
- Prediction results
Thanks
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