



Flash Memory Summit

The programmable Flash emulation system

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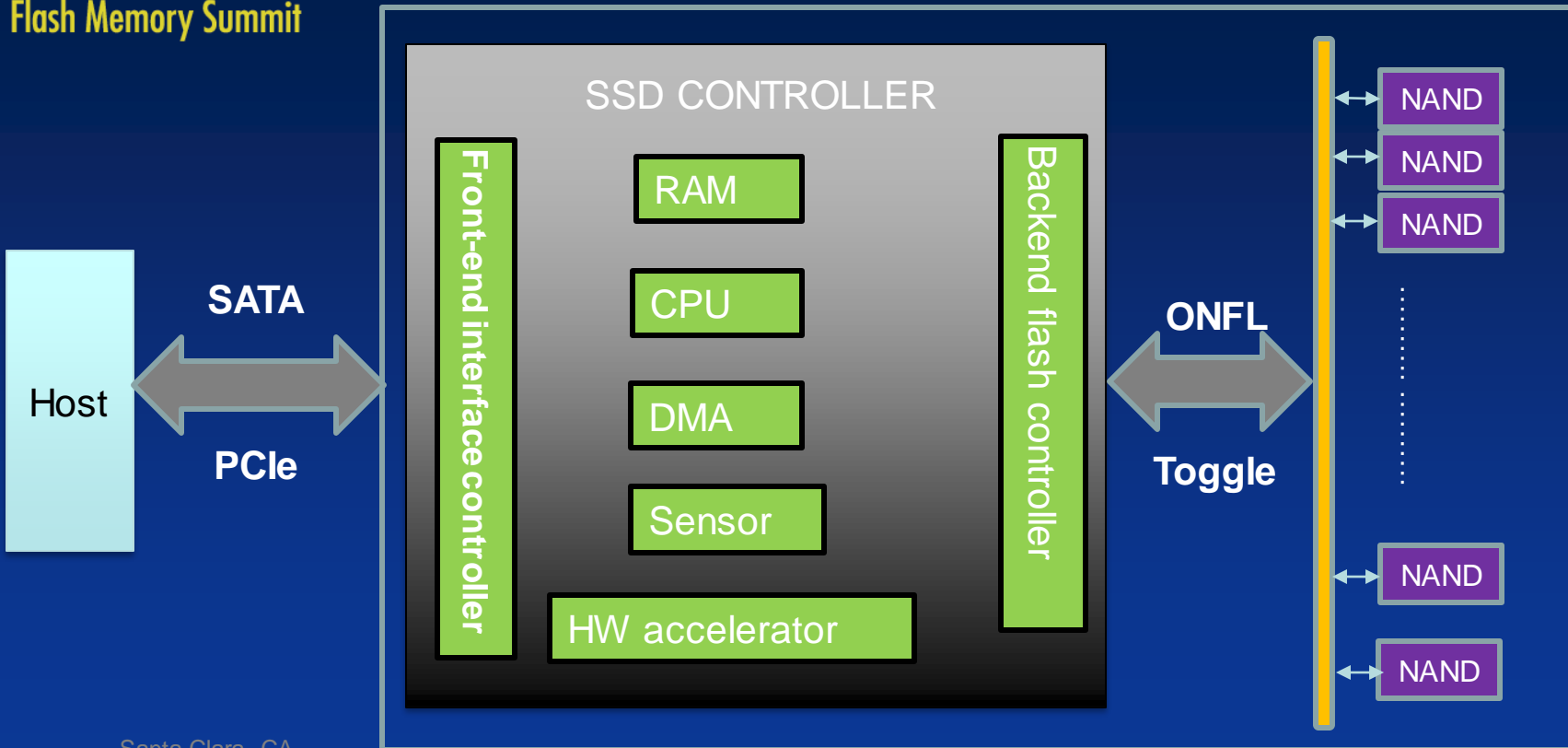
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The programmable Flash emulation system

- The Architecture of a typical SSD Controller
- The design target of Flash Controller
- Traditional verification method for Flash Controller
- The programmable Flash emulation system
- The BIT flip generator based on deep learning algorithm



Architecture of SSD Controller





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The design target of Flash Controller



**Interface
compatibility**



extension ability



**Exception handling
capability**



**Error correction
ability**



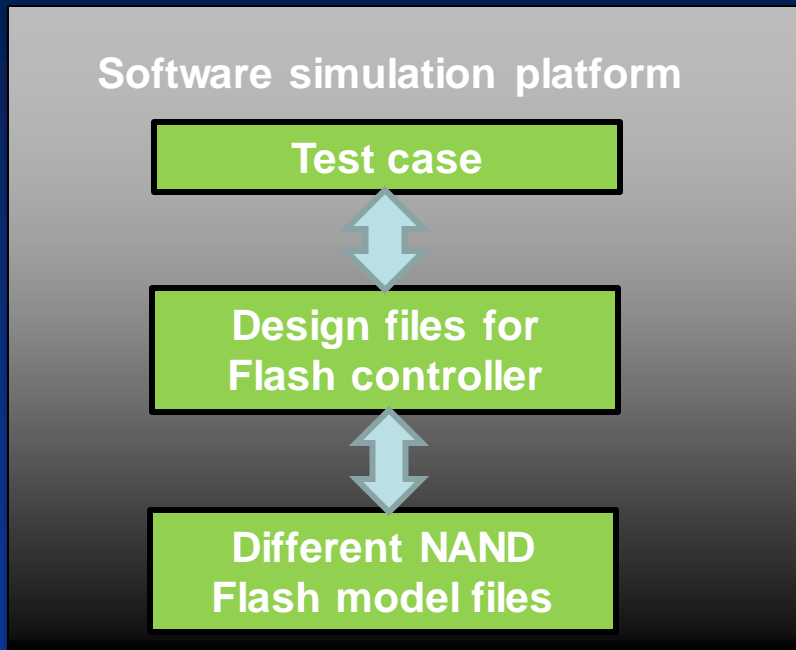
**Parallel processing
capability**



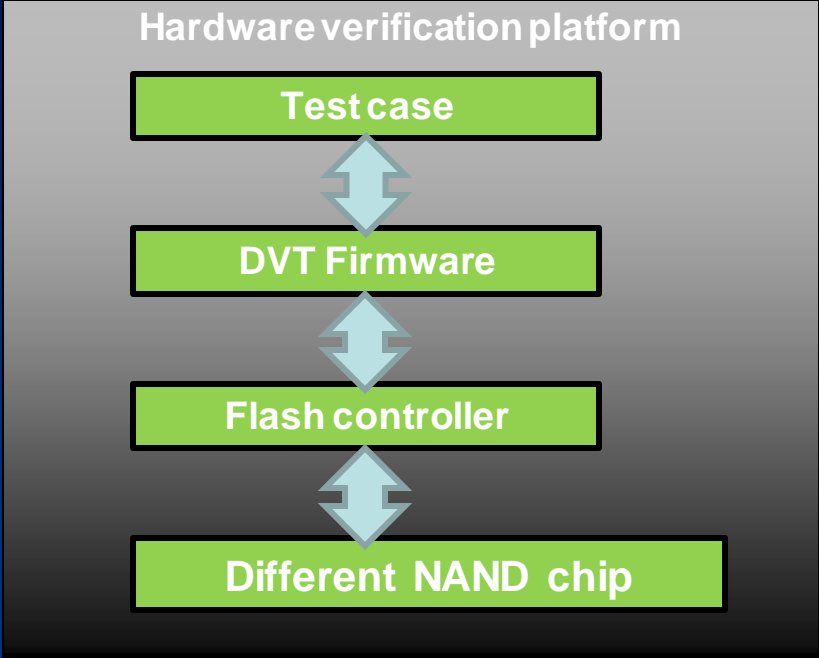
**Hardware and
software co-design**



Traditional verification method of Flash controller



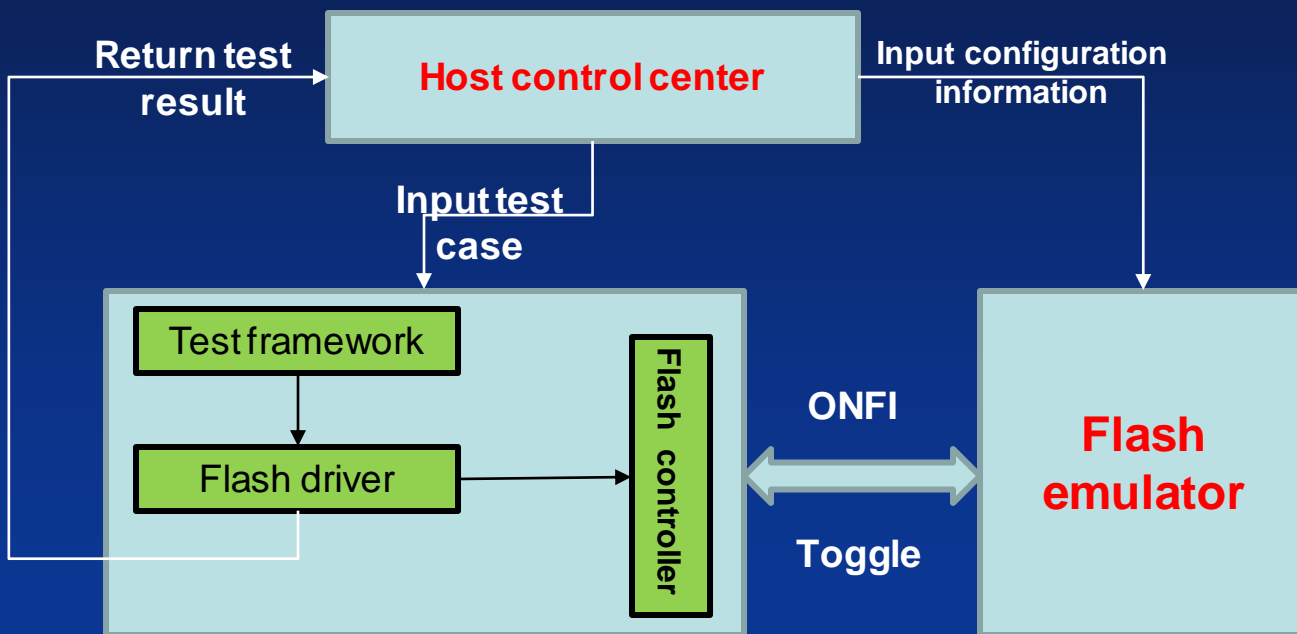
Software simulation verification



FPGA verification



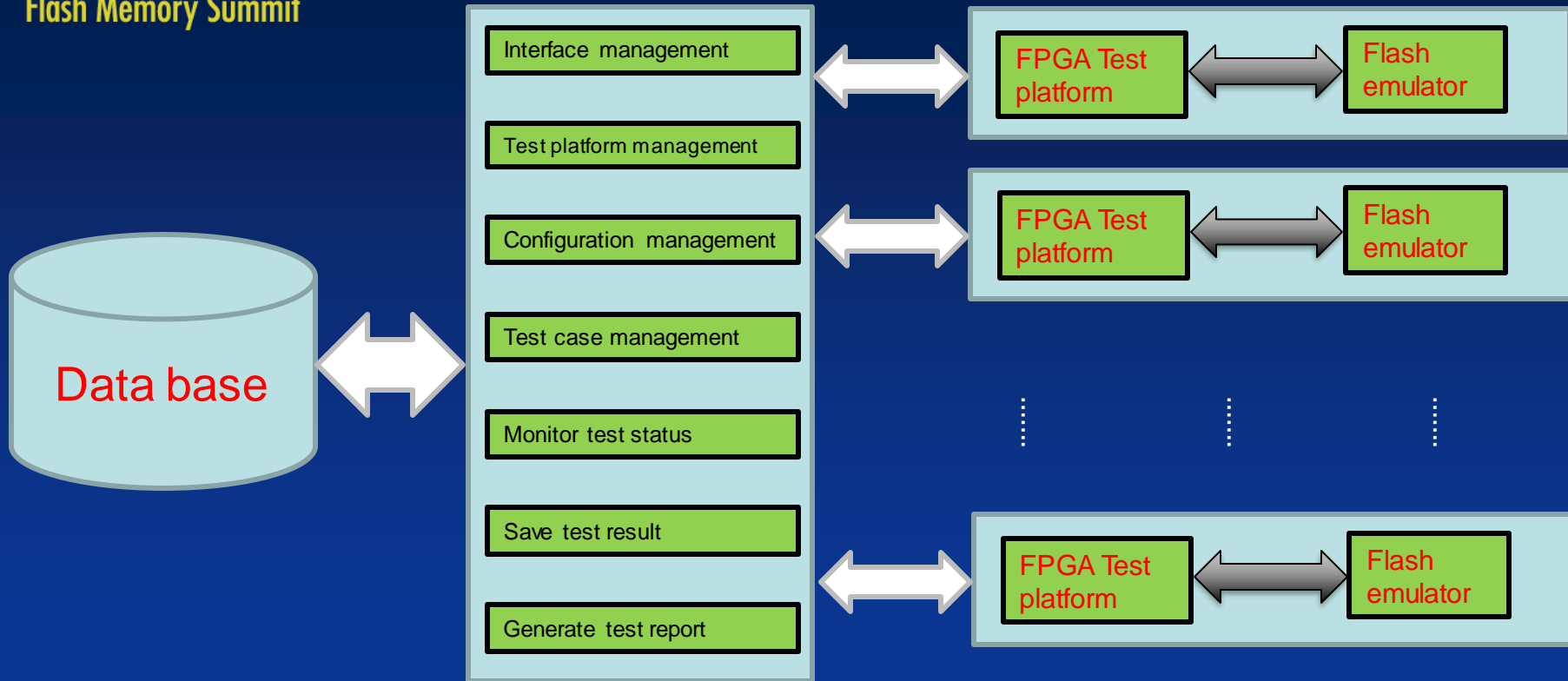
The programmable Flash emulation system



FPAG verification platform

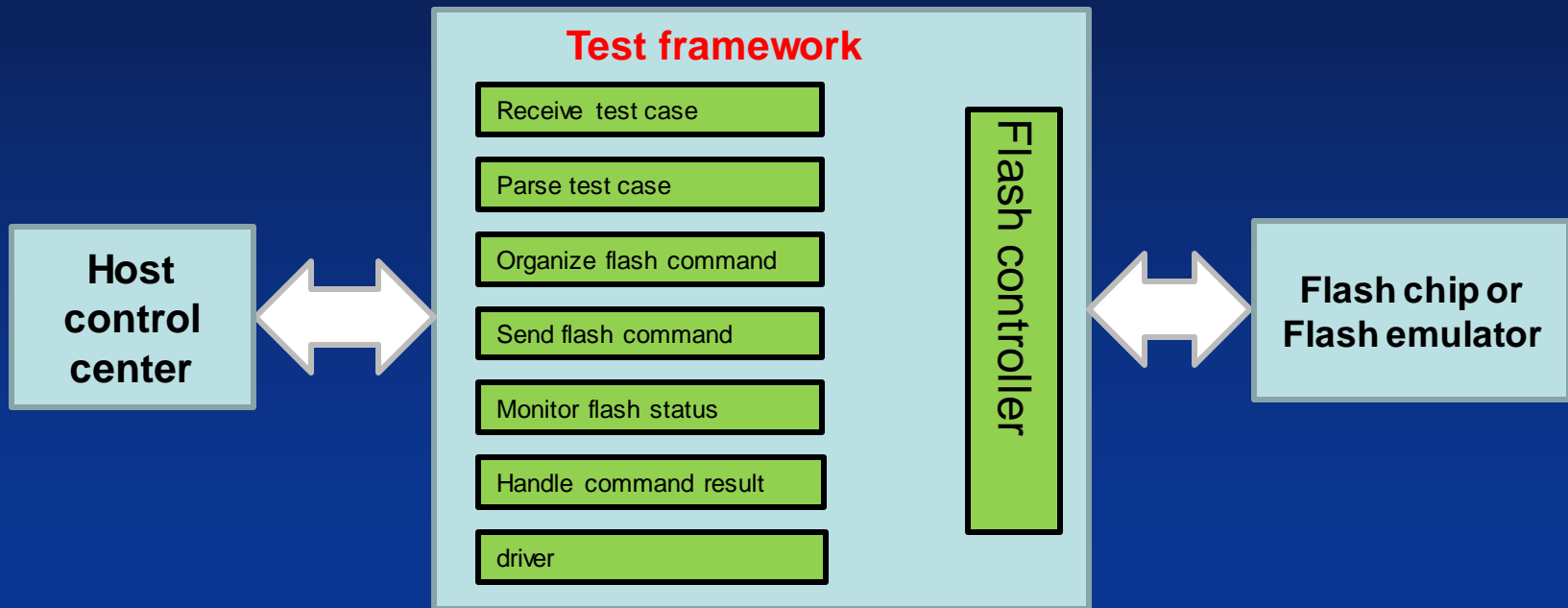


Host control center



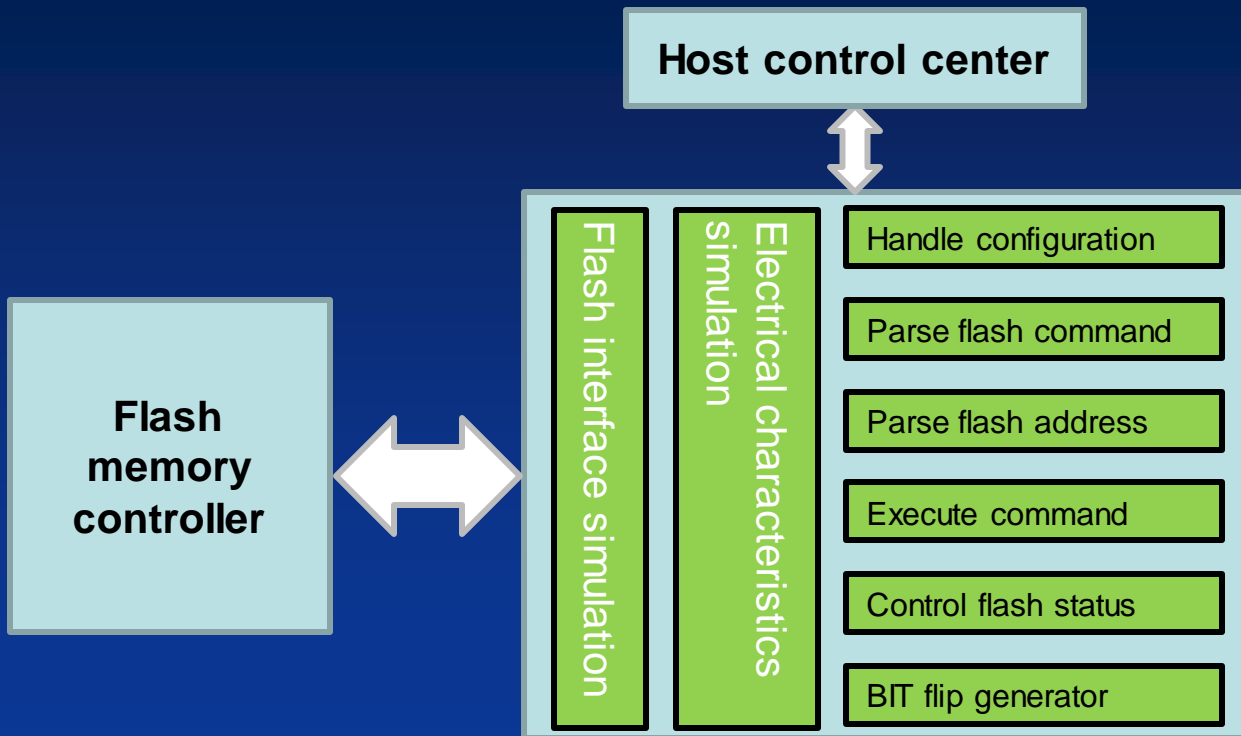


FPGA verification platform





Flash emulator



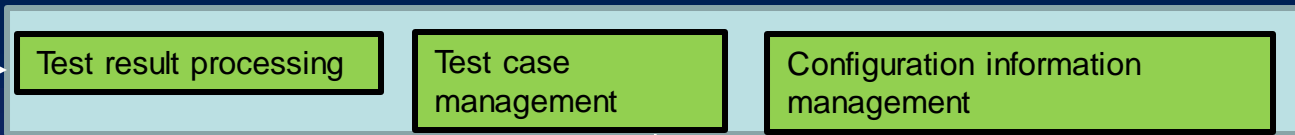
Flash emulator



The programmable simulation system

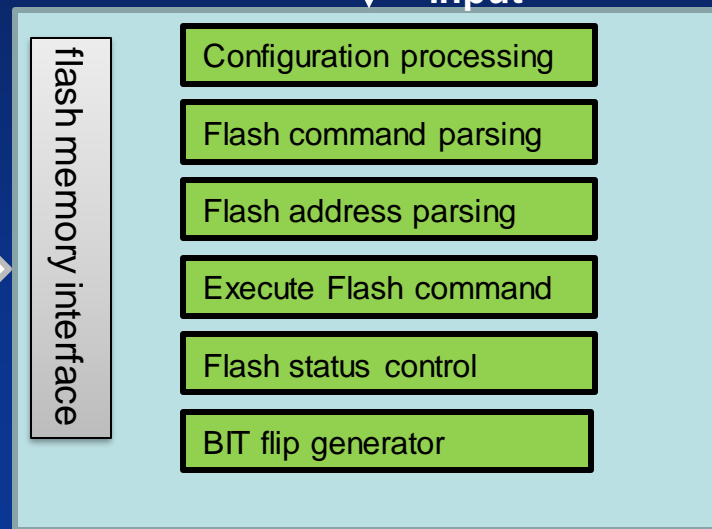
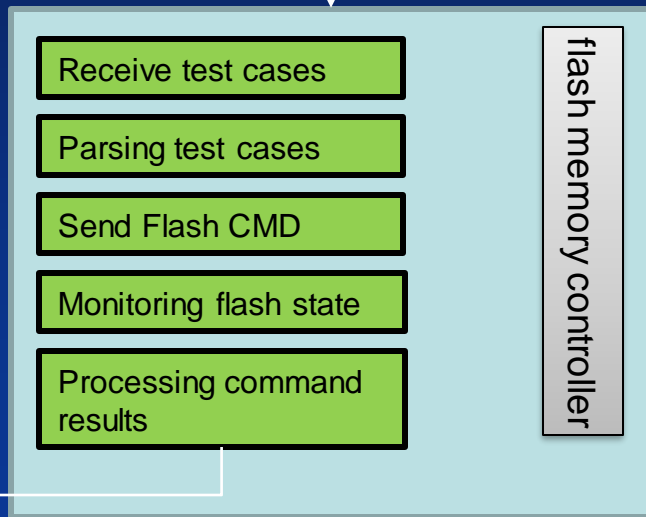
Host control center

Return test result



Test case input

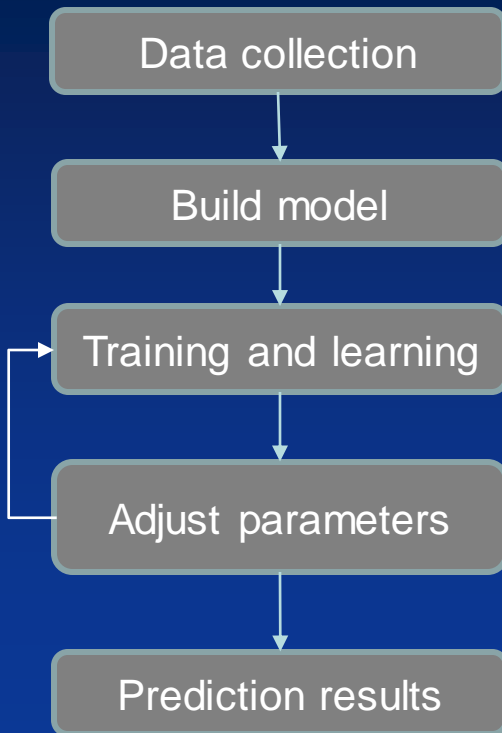
Configuration input





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The BIT flip generator based on Deep learning algorithm





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Thanks



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