An Advanced Flash Emulator for Designing Today’s High-Capacity Controllers

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University of Patras
Greece
Overview

- Why NAND Flash emulation at system level is needed?
- What are the challenges of emulation at system level?
- The architecture of NAND Flash Emulator
  - System Architecture
  - Memory Organization
  - Low-latency memory access
  - Experimental results
- Beyond the current NAND Flash Emulator
NAND Flash emulation at the system level

- **Storage devices**
  - Multiple memory ICs organized in channels
  - Multiple channels operating in parallel
  - Large memory capacity per channel (a few 10s or 100s GBs) – Huge capacity at system level (xTBs)
  - High IO rates and fast response time, especially when a page is read
  - Complicated functions (i.e. wear leveling, workload balancing) in the storage controller

- Full system prototyping and testing before the actual memory chips are available, based only on their specifications.
- Evaluate under different loading conditions the performance of the implemented algorithms
- Reduce time-to-market for the storage device when new memory chips become available

There is a need for an NAND Flash Channel Emulator that can emulate the whole memory capacity of a device and respond in real-time according to the NAND Flash specs.
The main challenges of a system Flash emulator

- **Emulate the whole system capacity**
  - Single board emulators have limited fast memory capacity (x10GBs)
  - Storage systems have multiple channels with multiple dies/channel and their total capacity ranges from x100GBs up to xTBs.

  **Solution:** Exploit the DRAM capacity of server motherboards
  - Directly accessed by the host processor, indirectly accessed by devices attached to PCIe slots
  - Access is affected by the used host processor (number of DRAM controllers, internal data paths)

- **Respond in real-time according the Flash IC specs**
  - Data access time in NAND Flash: 30 to 50 usecs and the page transfer time depends on the NAND Flash interface supported and the Flash page size.
  - Multiple channels operating in parallel generate asynchronous access requests
  - The latency introduced by the Operating System has to be avoided

  **Solution:** Use a fast PCIe-based FPGA board where the DUT is attached
  - Custom logic has to be developed for direct access to the host’s DRAM.
  - Modular design for supporting different Flash interfaces
Uses a low-cost commercially available motherboard that support the maximum possible DRAM (xTB)

Uses a PCIe card with a high-speed SoC FPGA that acts as the digital front-end to the DUT.

Modular re-usable system design

Split the design into two FPGAs boards, if needed.

- FPGA boards are interconnected using a High-Speed Digital Link (HSDL), i.e. xSFP+.

**Advantages:**

- Supports minimum latency, high capacity, various I/O NAND Flash interfaces and provides flexibility on the mechanical attachment of the DUT.

- Minimum additional development effort when new memory devices have to be supported.
NAND Flash Emulator Architecture

ONFI 1.0 - 3.0
50 - 400 MBps
Multiple CEs

ONFI Toggle etc.

I2C Control

DRAM Contr.

DRAM

Flash Cmds Processing Unit (FCPU)

Parameters RAM

Local Cmds Processing

Soft-CPU

Hardware Debugger Tracer

3CPU
Three (R/W/E) Commands Processing Unit

PCIe Controller (Gen.3, 8 lanes)

PCIe Switch

Emulated NAND Flash at Host DRAM (xTB)

Xeon Processor Ubuntu OS

SSD

PCIe Gen.3, 8/16 lanes

NFE Application Software

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Flash Memory Summit

PCIe Switch
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NAND Flash Emulator Software

Flash Memory Summit
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- ONFI Toggle etc.
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Flash Memory Summit
Data Flow in the NAND Flash Emulator

- Ubuntu
  - NFE Application Software
  - NFE Device Driver

- PCIe
  - 3CPU #0
  - 3CPU #1
  - Debugger Tracer
  - Local Memory
  - NFE Control (uB)

- Flash Cmds Processing Unit (FCPU)

- File
  - NFE Host Memory
Data Flow in the NAND Flash Emulator

Ubuntu

NFE Application Software

NFE Device Driver

NFE Host Memory

File

PCle

3CPU #0

3CPU #1

Debugger Tracer

Local Memory

NFE Control (uB)

Flash Cmds Processing Unit (FCPU)

CH-0

CH-1
Data Flow in the NAND Flash Emulator

Ubuntu

NFE Application Software

NFE Device Driver

File

NFE Host Memory

NFE Control (uB)

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Flash Cmds Processing Unit (FCPU)

PCIe

3CPU #0

3CPU #1

Debugger Tracer

File

Flash Memory Summit 2018
Santa Clara, CA
Data Flow in the NAND Flash Emulator

- Ubuntu
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- NFE Device Driver
- File
- NFE Host Memory
- PCIe
- 3CPU #0
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- Debugger Tracer
- Local Memory
- NFE Control (uB)
- Flash Cmds Processing Unit (FCPU)
- CH-0
- CH-1

Data Flow in the NAND Flash Emulator

Flash Memory Summit 2018
Santa Clara, CA
Memory Organization and Emulator Capabilities

2 channels, 4 dies/channel
Memory Organization and Emulator Capabilities

<table>
<thead>
<tr>
<th></th>
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<td>4.22</td>
<td>5.0</td>
<td><strong>107.3 M</strong></td>
<td>64</td>
<td>64</td>
<td>16 – 4</td>
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<tr>
<td>8.0</td>
<td>8.44</td>
<td>9.0</td>
<td><strong>59.6 M</strong></td>
<td>128</td>
<td>32</td>
<td>8 – 4</td>
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<tr>
<td>16.0</td>
<td>17.25</td>
<td>18.0</td>
<td><strong>29.8 M</strong></td>
<td>256</td>
<td>16</td>
<td>4 - 4</td>
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<tr>
<td>16.0</td>
<td>18.16</td>
<td>19.0</td>
<td><strong>28.2 M</strong></td>
<td>512</td>
<td>8</td>
<td>4 - 2 or 2 - 4</td>
</tr>
</tbody>
</table>

512 GB emulated NAND Flash  (DRAM: 576 up to 640 GB)
Prototype of the NAND Flash Emulator

**HTG-K800**
Xilinx Kintex UltraScale KU085

Emulates up to
- 2 NAND Flash channels
- 4 - 8 CE per channel
- 2 GB L1 cache
- Specs
  - ONFI 1.0 - 3.0
  - Toggle 1.0 - 2.0

<table>
<thead>
<tr>
<th>DIMM capacity</th>
<th>Total DRAM</th>
<th>DRAM for NFE</th>
<th>Emulated NAND Flash Memory</th>
</tr>
</thead>
<tbody>
<tr>
<td>64 GB</td>
<td>512 GB</td>
<td>496 GB</td>
<td>480 GB</td>
</tr>
<tr>
<td>128 GB</td>
<td>1 TB</td>
<td>768 GB</td>
<td>656 GB</td>
</tr>
</tbody>
</table>
NAND Flash Emulator Software

**DRAM Initialization**

1. NAND Flash IC
2. SSD
3. DRAM

**Operation**

1. Emulator initialization
2. Start
3. Status update
4. End

**Log/tracing info**

- NAND Flash parameters
- Emulator initialization

**Flash Memory Summit**

[Image of a computer motherboard]
3CPU and Tracer Architecture

DMAs data width: 16 up to 128 bits
NAND Flash Emulator - Timing

**Timing**

- **Page size [B]**
- **Read Time [usecs]**
- **Write Time [usecs]**
- **ONFI**
- **Transfer Rate [MBps]**
- **Transfer Time [usecs]**
- **Transfer Time over PCIe (8 lanes Gen3, 128 bits DMA) [usecs]**
- **NAND Flash Channels supported**

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</tr>
</thead>
<tbody>
<tr>
<td>8,640</td>
<td><strong>50</strong></td>
<td>1,300</td>
<td>2.0</td>
<td>166</td>
<td>52.0</td>
<td><strong>2.6</strong></td>
<td><strong>18</strong></td>
</tr>
<tr>
<td>8,640</td>
<td><strong>35</strong></td>
<td>300</td>
<td>2.2</td>
<td>200</td>
<td>43.2</td>
<td><strong>2.6</strong></td>
<td><strong>12</strong></td>
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<tr>
<td>18,592</td>
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<td>1,400</td>
<td>3.0</td>
<td>166</td>
<td>112.0</td>
<td><strong>5.1</strong></td>
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<td>18,592</td>
<td><strong>50</strong></td>
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<td>333</td>
<td>55.8</td>
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**Flash IF**

- **35 – 50 usecs**
- **40 – 140 usecs**
- **50 - 400 MBps**

**FCPU**

- **2.6 – 5.1 usecs**
- **up to 6 GBps**

**3CPU**

**PCIe**

- **Flash Memory Summit**
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3CPU Experimental Results

17,408 B/page
128 pages/block
Tracer Performance

16 GB at Host DRAM
Multiple-channels NAND Flash emulator characteristics:

• Supports a large number of NAND Flash channels
• Practically supports unlimited NAND Flash Capacity
• Responds according to the NAND Flash chips
• Supports ONFI and Toggle interfaces
• Due to its modular design can be re-used for emulating other Non-volatile Memory (NVM) technologies and/or other IO interfaces (i.e. eMMC)
• Design of new algorithms based on data analytics (i.e. minimize read latency by predicting future read/write commands)
Thank you for your attention!

Questions?

http://www.loe.ee.upatras.gr/English/COMES-home.htm
Back-up slides
NAND Flash Emulator

Single board configuration

Two boards configuration

x10Gbps

GbE
Emulation using a cluster of servers - case #1

Single server cannot support the capacity of the storage device
Emulation using a cluster of boards

Single DFE cannot support the number of channels of the storage device
Emulation using a cluster of servers - case #2
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Xeon E5-2650 v4
HTG-K800
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