FeFET Memory: (e)NVM for Advanced Technology Nodes

Dr. Stefan Müller (Ferroelectric Memory Co.)
FeFET is not FRAM!

What I am not going to talk about:
Classical 1T-1C FRAM

1T-1C memory cell
Exotic ferroelectric materials (PZT)
Stuck at 130 nm

What I am going to talk about:
Novel 1T FeFET

1T memory cell
Ferroelectric HfO₂
In dev. at 22 nm

THE enabler for FeFET!

Source: Science, Vol. 315, pp. 954-959

30 nm W Poly TiN Si:HfO₂ Silicon
Ferroelectric HfO$_2$

Amorphous (unordered) HfO$_2$
(used in CMOS gate stack)

Crystalline (ordered) HfO$_2$
(used in DRAM capacitor)

*Actually ZrO$_2$ but chemically almost identical

Discovery (2007)

Ferroelectric HfO$_2$
2 atom positions = 1 Bit!
(Patented)

Dr. Stefan Müller (CEO)
Why it matters

Planar transistor (> 20 nm)

Fin-transistor (20 nm – 7 nm, today)

Nanowire-transistor (< 7 nm, future)

We transform any logic transistor into a memory cell! (2 threshold voltage states)
FeFET vs. eFlash

**FeFET:**
- 2 additional masks
- Write voltage 2V ... 4V
- Write by gate voltage only

**eFlash (2 bit):**
- 15+ additional masks
- Write voltage > 10V
- Write by channel current flow (HCI)
FeFET vs. emerging NVM

Emerging NVM (RRAM, MRAM, PCM)

The FeFET solution

Challenges:
- Additional memory element R adds cost!
- Higher power consumption
- Questionable scalability

FeFET benefits:
- Reduces manufacturing cost significantly
- Lowers power consumption by 1000x
- Inherently scalable alongside CMOS
# Technology status

<table>
<thead>
<tr>
<th></th>
<th>FeFET array (IEDM ‘16 &amp; ‘17)</th>
<th>Lab capacitor</th>
<th>Theory</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Cell size</strong></td>
<td>44F² (0.035 µm²) planar AND-type</td>
<td>&gt; 10,000 µm²</td>
<td>&lt; 4F² (3D)</td>
</tr>
<tr>
<td><strong>Write speed</strong></td>
<td>10 ns</td>
<td>10 ns</td>
<td>&lt; 1 ns</td>
</tr>
<tr>
<td><strong>Read speed</strong></td>
<td>20 ns (limited by design)</td>
<td>10 ns</td>
<td>&lt; 1 ns (architecture)</td>
</tr>
<tr>
<td><strong>Endurance</strong></td>
<td>10⁵ cycles</td>
<td>&gt; 10¹⁰ cycles</td>
<td>Unlimited</td>
</tr>
<tr>
<td><strong>Retention</strong></td>
<td>250° C / 7 days (0.28 µm² cell)</td>
<td>10y at 125° C extr.</td>
<td>10y at &gt; 175° C</td>
</tr>
<tr>
<td><strong>V&lt;sub&gt;write&lt;/sub&gt;</strong></td>
<td>4 V</td>
<td>1.5 V</td>
<td>~ 1V</td>
</tr>
<tr>
<td><strong>Write energy</strong></td>
<td>&lt; 1fJ (per bit)</td>
<td>&lt; 1fJ (per bit)</td>
<td>Below fJ</td>
</tr>
<tr>
<td><strong>Mask set adder</strong></td>
<td>2</td>
<td>NA</td>
<td>1</td>
</tr>
<tr>
<td><strong>Tool capex</strong></td>
<td>No</td>
<td>No</td>
<td>To be discussed</td>
</tr>
<tr>
<td><strong>Solder reflow</strong></td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
</tbody>
</table>
Impact on memory landscape

FE-HfO₂-based:

- Proof-of-concept
- Arrays / circuits
- Qualification
- Product

SRAM/DRAM
FRAM
eNVM
SSD / SCM

DRAM vendors / foundries / IDMs

DRAM vendors

3D NAND vendors

J. Müller et al., ECS, 2015.
3D capability of FE-HfO₂
Beyond 60mV/dec
Cross-point capability
Derived from DRAM
New application space
Embedded capability
Capacitor cost adder

K. S. Li et al., IEDM, 2015.
Market (150 billion US$)
Relaxed wrt statistics
Ultimate application
Similar hurdles as for NVM FeFET
Epitaxial film required

"Universal" memory

BEOL
BEOL
No 3D capacitor required
FE-HfO₂ thickness limit?
Access device?
Epitaxial film required

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Flash Memory Summit 2018
Santa Clara, CA
Thank you!

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