Emerging NVM Features

For Emerging NVM Interface (I/F)s
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Introductions

- Thomas Won Ha Choi – Senior Engineer, SK hynix
  - DRAM Server Product Planning
  - Specialties:
    - Standardization (JEDEC, Emerging Open Interconnect)
    - Future Memory Pathfinding / System-level Performance Analysis
    - Persistent Memory (PM) Interfaces
  - B.S. in Computer Sciences from Univ. of Texas at Austin
  - M.S. in Computer Engineering from Univ. of Southern California
  - Ph.D. in Computer Engineering from North Carolina State Univ.
  - Worked in Advanced Design / Product Planning at SK hynix since 2012
Objectives of Emerging NVM HW

- “Storage Class” High Capacity
- Persistent Memory (i.e. byte-addressable)
## Key Features of Emerging NVM HW

- Persistent Features & Memory Protocol on High Speed I/F
- Form factors may vary by customer requirements

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<td>NVDIMM-P: up to 40-bit space</td>
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<td>Non-deterministic, transactional protocol</td>
<td>Handshaking signal, write credit, status check</td>
<td>NVDIMM-P: integrated in DDR4/5 protocol</td>
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<td>Byte-addressable Persist Command</td>
<td>FLUSH, PWRITE</td>
<td>Flush supported in various emerging NVM I/Fs</td>
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<td>RAS related</td>
<td>Error correction &amp; reporting, media management</td>
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<td>Power/thermal management</td>
<td>Power throttling, interrupt, failure &amp; reset handling</td>
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<td>Security</td>
<td>Encryption</td>
<td>May be agnostic to I/F</td>
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Choosing I/Fs and Form Factors

- Customer demand will drive the leading I/F & Form Factor (FF)s
  - Based on cost, scaling (capacity, BW, power)
  - I/F choices:
    - JEDEC NVDIMM-P (DDR5)
    - Emerging Open Interconnect (CCIX, Gen-Z, OpenCAPI)
    - Proprietary I/F
  - FF choices:
    - DIMM
    - SSD (U.2., EDSFF, etc.)

Less per-bit cost than DRAM DIMMs, higher bandwidth, but less tolerable power budget (15~18W) and more stacking required for capacity scaling.

More tolerable power budget (~25W), less stacking required for capacity scaling, but more per-bit cost than NAND SSDs.
Example I/F: NVDIMM-P

- Non-deterministic, transactional PROTOCOL on DDRx bus
- Expanded capacity:
  - Only 2 clock cycle added to existing read/write command (ex: DDR5)
- Transaction Flow:
  - Read: Read command -> Read ready -> SEND data -> data out
  - Write: Write command if enough write credit -> handshaking only for persistent writes
- Guaranteeing data preservation
  - Persistence command, RAS
  - Security (TBD)
NVDIMM-P Persist Command

- PWRITE or FLUSH command with non-deterministic, transactional protocol
- FLUSH overrules prior PWRITEs
NVDIMM-P RAS Features

- Status of NVDIMM-P can be polled at command level (SEND command)
- Other RAS features: channel ECC, IOP, UNMAP

**Command**

SEND

**DQ**

- tSEND

**ECC + Metadata**

- Normal read data OR status metadata (PWRITE related, IOP related, etc.)
- Check Bit (CB) not stored in NVDIMM-P media
- 1-Symbol (8-bit) correct, 2-symbol detect
- Basic metadata (RID, Write credit, user metadata, etc.)
NVDIMM-P Form Factor

- Expected to follow 288-pin LRDIMM form factor (with RCD, DB)

- Two separate trainings conducted: media controller & media:
  - Host is still expected to have control of media controller training
  - Control word combines two separate registers currently in DDRx:
    - RCW (Register Control Word) in RCD
    - MR (Mode Register) in media component

- Power requirement: under 15W (current R/LRDIMM budget)
  - Some argue that up to 18W is acceptable
Conclusion

- Emerging NVM HW targets high capacity and persistent memory.

- Emerging NVM I/F standardization efforts are currently defining persistent memory command, RAS, power/thermal management, and security features.

- Become more active in standardization efforts for more exciting future, including JEDEC NVDIMM-P!
Thank You!

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