UFS 3.0 - Controller Design Considerations

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Before I Start....

1. What’s the benefit of adopting UFS?
2. What’s the UFS application/market?

What’s the UFS3.0 requirements that controller company need to consider?
Mobile Storage Evolution

- eMMC
  - Latest widely adopted standard before UFS 2.x
  - Limited to 400MB/s (duplex) since 2013

- UFS 1.x
  - Not adopted

- UFS 2.x
  - Offers desktop-grade performance of ~1200MB/s over full-duplex links
  - Good adoption in flagship devices (2017)

- UFS 3.0
  - Doubles UFS 2.x performance, offering ~2400MB/s
  - Requirements are tough for mobile form factors
1. High Throughput

2. Low Active Power

3. Low Latencies

4. Cost Management
   a) Reduced DIE Size
   b) Support to latest 3D NAND technologies
UFS 3.0 Controller Requirements

1. High Throughput
2. Low Active Power
3. Low Latencies
4. Cost Management
   a) Reduced DIE Size
   b) Support to latest 3D NAND technologies
UFS 3.0 Controller Challenges

High Speed Host Interface
12Gbps per Lane

Full control over the IP design allowing for optimization

Design with packaging in mind to avoid Signal Integrity issues

Reduce IP Area and Power Consumption
UFS 3.0 Controller Requirements

1. High Throughput
2. Low Active Power
3. Low Latencies
4. Cost Management
   a) Reduced DIE Size
   b) Support to latest 3D NAND technologies
UFS 3.0 Controller Challenges

- High Speed Flash Interface
- High Speed Error Correction Engine
- Hardware Acceleration to reduce FW & CPU Overhead
- QoS (Quality of Service)

Having in-house IPs can shape the design around these requirements
UFS 3.0 Controller Requirements

1. High Throughput

2. Low Active Power

3. Low Latencies

4. Cost Management

   a) Reduced DIE Size

   b) Support to latest 3D NAND technologies
Newer Process: All About the Right Balance
## Choosing the Ideal Process

<table>
<thead>
<tr>
<th></th>
<th>Phison Gen1</th>
<th>Phison Gen2</th>
<th>Next Gen</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Application</strong></td>
<td>UFS 2.1 - HS G3 x1-L</td>
<td>UFS 2.1 - HS G3 x2-L</td>
<td>UFS3.0 - HS G4 x2-L</td>
</tr>
<tr>
<td><strong>ECC Throughput</strong></td>
<td>800MB/s (800 x1)</td>
<td>1333MB/s (800 x1.66)</td>
<td>2666MB/s (800 x3.33)</td>
</tr>
<tr>
<td><strong>Area (aprox.)</strong></td>
<td>x1</td>
<td>x0.32</td>
<td>x0.44</td>
</tr>
<tr>
<td><strong>Power Consumption</strong></td>
<td>x1</td>
<td>x0.46</td>
<td>x0.67</td>
</tr>
<tr>
<td><strong>DIE Area Cost</strong></td>
<td>x1</td>
<td>x0.53</td>
<td>x0.75</td>
</tr>
</tbody>
</table>

A newer process will bring more advantages. However mask investment, wafer cost, production schedule, IP availability (if not in-house) will have to be considered.
In device controller design, the balance between performance, power and cost is critical. A total control of the design will offer more flexibility to optimize the solution.

In-house IPs can optimize the cost and requirements
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<table>
<thead>
<tr>
<th>Performance</th>
<th>PS8313* 3D TLC</th>
<th>PS8313* 3D TLC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Host Interface Mode</td>
<td>HS-Gear 3B x1 Lane (eUFS / UFS Card)</td>
<td>HS-Gear 3B x2 Lanes (eUFS only)</td>
</tr>
<tr>
<td>NAND Flash Configuration</td>
<td>2ch, 4CE @667MT/s</td>
<td>2ch, 4CE @667MT/s</td>
</tr>
<tr>
<td>Seq Read</td>
<td>530 MB/s</td>
<td>920 MB/s</td>
</tr>
<tr>
<td>Seq Write</td>
<td>400 MB/s</td>
<td>550 MB/s</td>
</tr>
<tr>
<td>Random Read</td>
<td>67,000 IOPS</td>
<td>67,000 IOPS</td>
</tr>
<tr>
<td>Random Write</td>
<td>60,000 IOPS</td>
<td>62,000 IOPS</td>
</tr>
</tbody>
</table>

*Test with Phison Tester (No host/OS overhead)
Thank you