A Novel On-the-Fly NAND Flash Read Channel Parameter Estimation and Optimization

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Flash Memory Summit 2017
Santa Clara, CA

Outline

- Significance of flash read channel parameters
- Overview of existing methods
- Novel on-the-fly read sensing threshold estimation
- Experimental results
- Summary

Legacy NAND Challenges

- Process uniformity and defects
- Gradual wear
- Data retention
- Program disturb
- Read disturb
- Wide range of working temperature
- …

Emerging 3D NAND Challenges

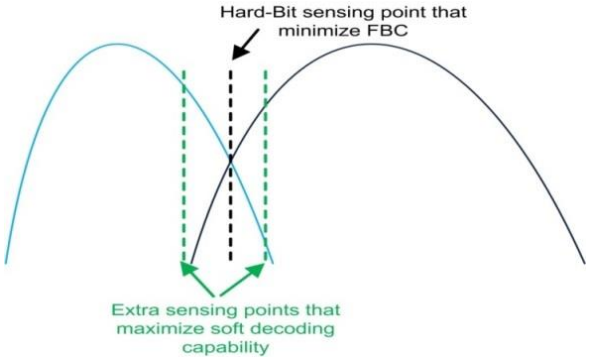
- New characteristics
- Large process variations
- QLC denser packings
- Ever increasing performance and endurance requirements

Flash Read Channel Parameters Are Vital

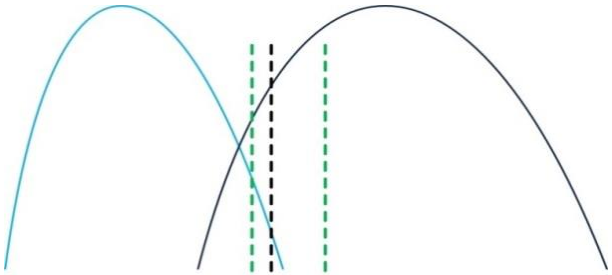
- Flash read channel parameters:
  - Sensing points
  - Corresponding Log-Likelihood Ratio (LLRs)
- Narrower Vt window size
  - more prone to high FBC
- Die-to-die, block-to-block, page-to-page variations
  - Need self-adaptive read threshold optimization method
- Greatly impacts quality of service (QoS): throughput, latency and endurance

Illustration of Flash Read Parameters

- Good read thresholds
  - Hard decoding FBC minimized
  - Corresponding LLR optimized
  - Soft Decoding capability maximized



- Bad read thresholds
  - Hard decoding FBC worsened
  - Suboptimal extra sensing points
  - Soft decoding performance compromised



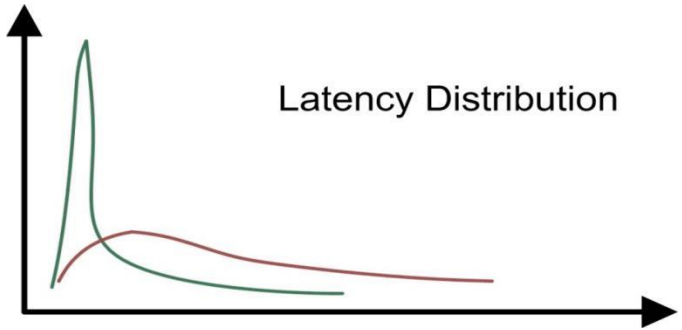
Existing Methods for Estimating Read Thresholds

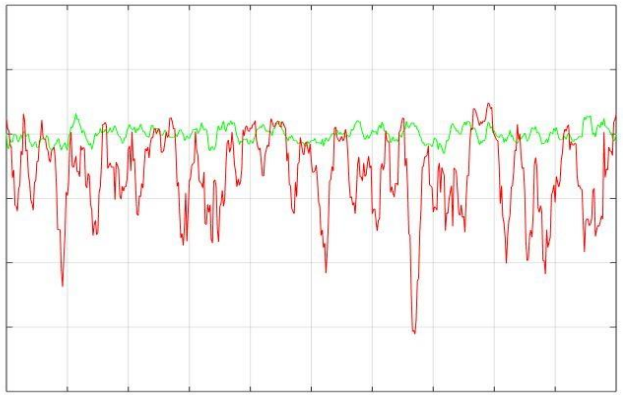
- Offline Characterization
  - Fixed values of sensing points
  - Fixed values of Log-likelihood Ratio (LLR)
  - Can not well adapt to process variations
  - Usually degraded decoding performance, latency and endurance

- Decision Feedback Based Methodology
  - Complicated interactive mechanism between modules
  - High complexity and handling cost
  - Sometimes ECC dependent

Effects of Flash Read Parameters on QoS

Comparison of System Latency →





← **Comparison of System Throughput**

: Optimized Flash Read Parameters

: Inferior Flash Read Parameters

Design Objectives

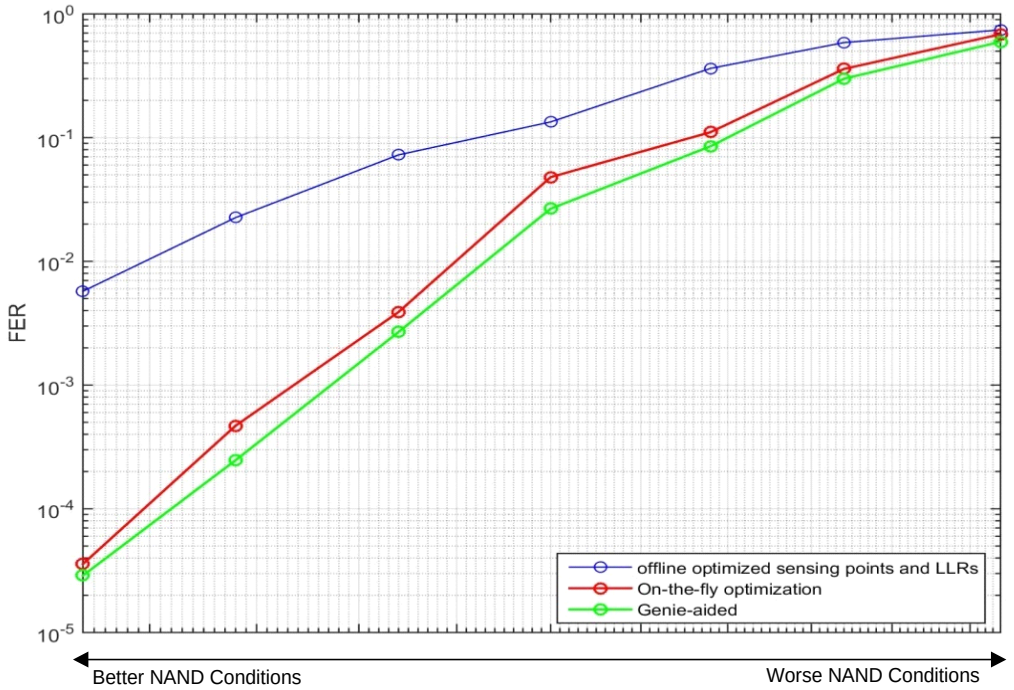
- On-the-fly identify optimized sensing points and LLRs
- Self-adapt to volatile NAND conditions
- Increase Hard/Soft decoding error correcting capability
- Enhance SSD system quality of service (QoS)
  - Throughput
  - Latency
  - Endurance

Proposed Algorithm Features

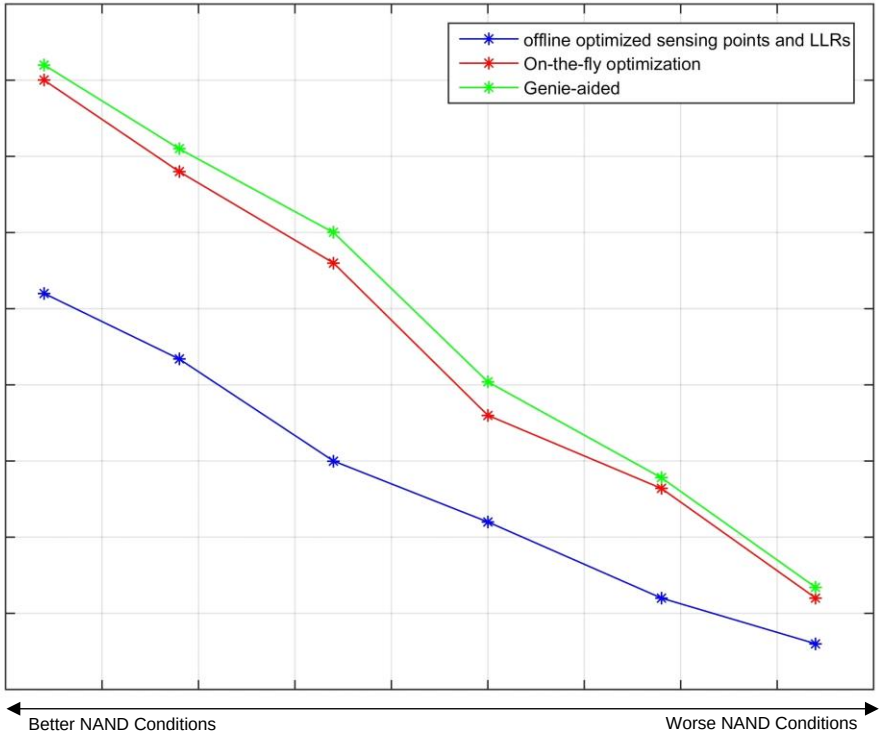
- Low-complexity (online estimation)
- Self-adapt to converge at optimized sensing points and LLRs
- Highly robust to asymmetric distribution cases
- ECC independent
- Flexible configurations for the improvement/complexity tradeoff
- Decision feedback is minimal

Experimental Results

- 1KB codelength LDPC with rate=0.9



Throughput Comparison

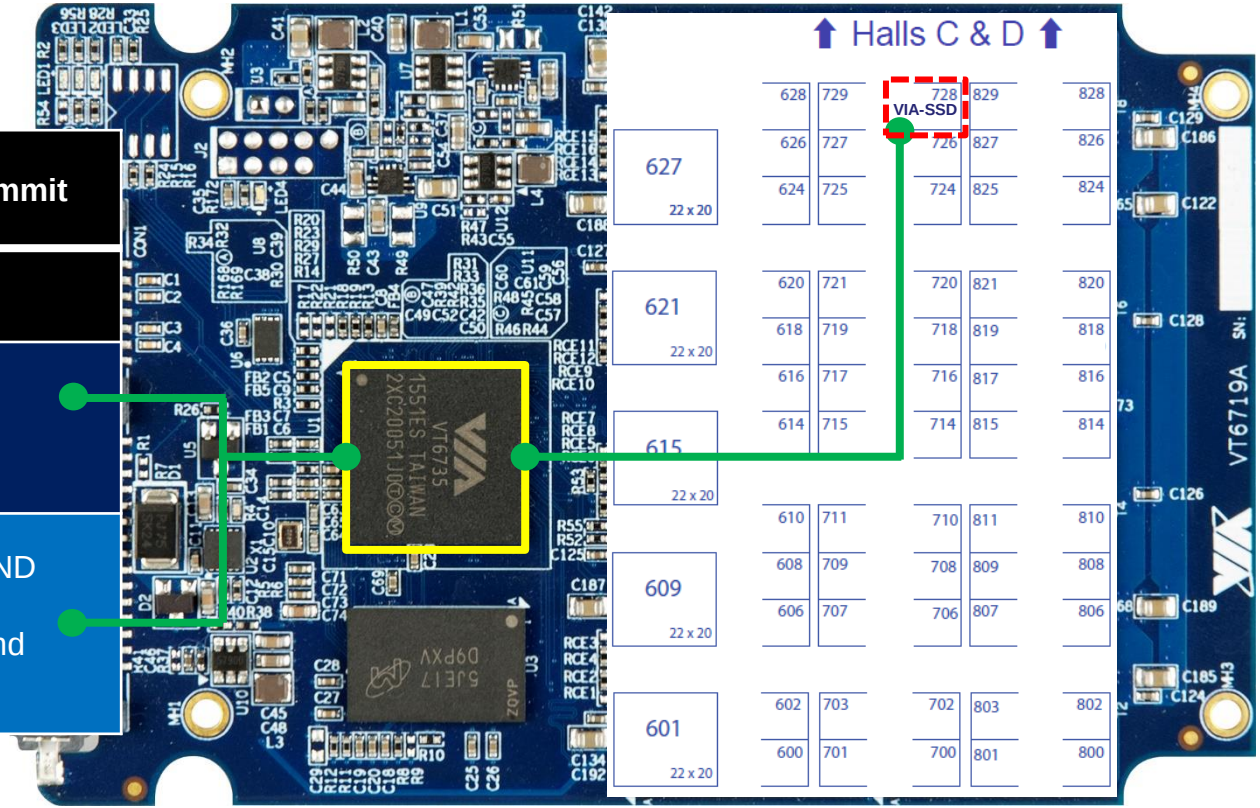


Summary

- Flash read parameters play a vital part in the state-of-art SSD system
  - Greatly affects SSD throughput, endurance and latency

- On-the-fly estimation and adjustment of optimized sensing points and LLRs
  - Based on mass distribution from NAND sensing results
  - Low-complexity and self-adaptive solution
  - Independent of ECC schemes and NAND types
  - Effectively improves system performance

- VIA Flash Management Technology takes every possible measure to care for the delicate 3D-NAND flash.

We Are @ Booth #728

VIA Technologies @ Flash Memory Summit	
Time	Presentation
Forum E-22 Wed, Aug. 9 3:20 ~ 5:45pm	Power Efficient LDPC Technology for High Performance SSDs
Forum M-22 Wed, Aug. 9 3:20 ~ 5:45pm	A Novel On-The-Fly NAND Flash Read Channel Parameter Estimation and Optimization