



Overcoming Challenges in 3D NAND Volume Manufacturing

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Vice President, Etch Emerging Technologies and Systems

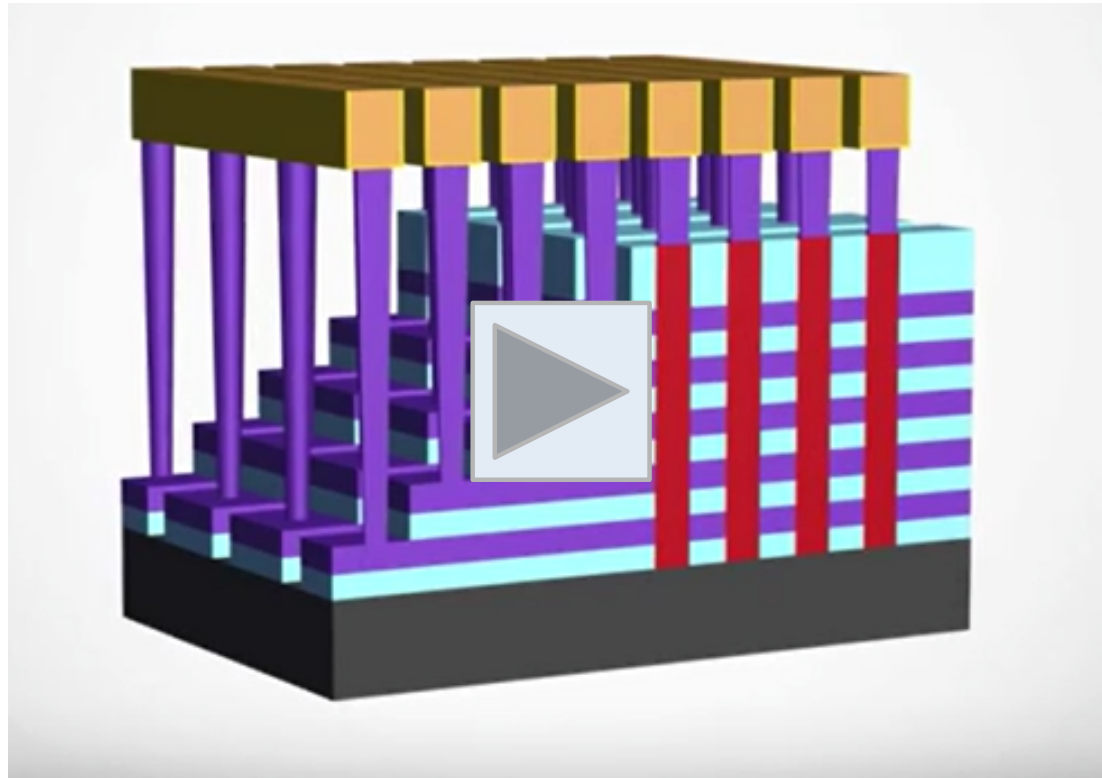
Flash Memory Summit 2017, Santa Clara



Topics Introduction

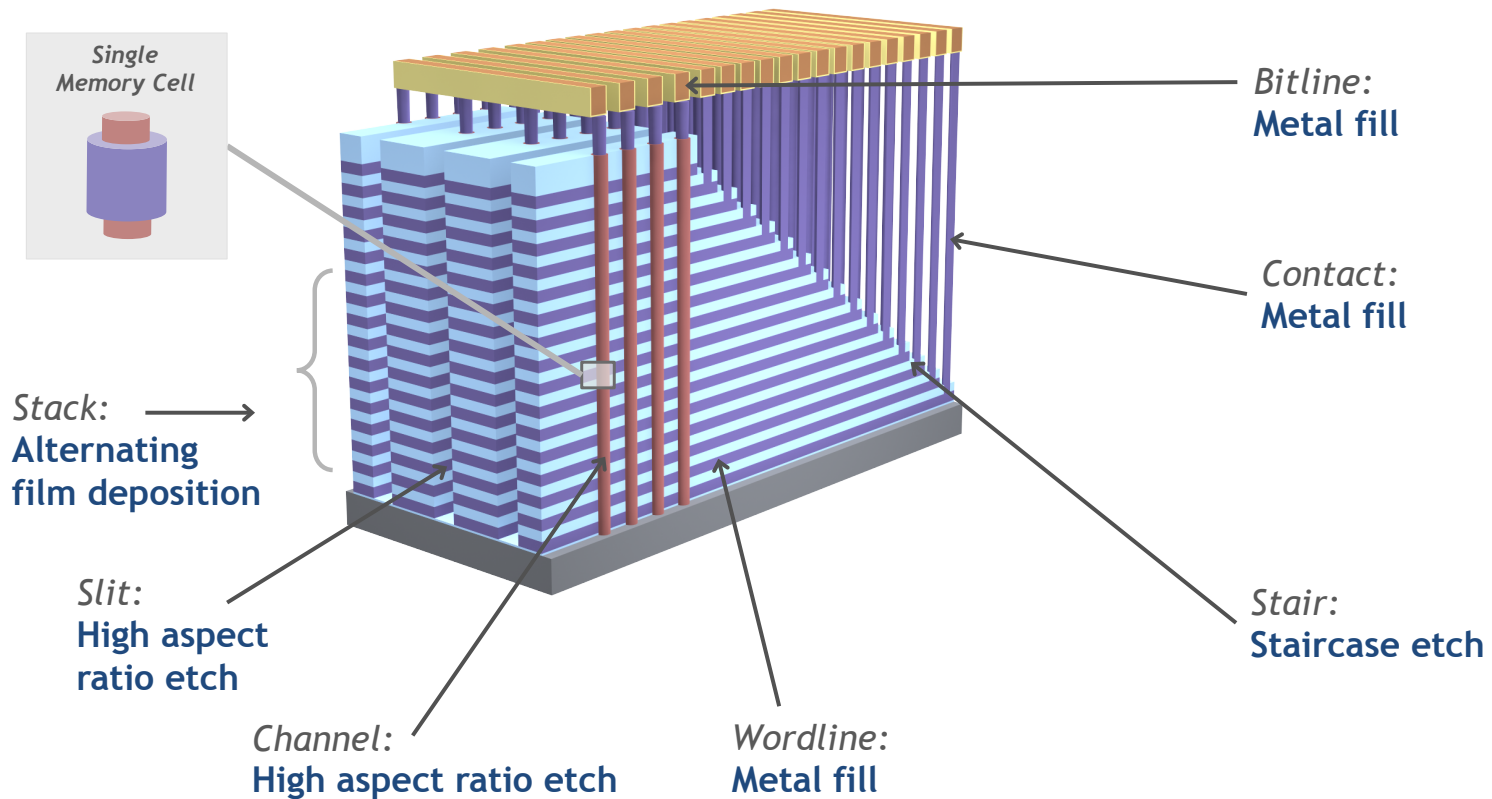
- ▶ Video showing 3D NAND manufacturing process
- ▶ Etch and deposition process challenges and solutions for 3D NAND
- ▶ Process control on-tool solutions
- ▶ Summary

Deposition and Etch Processes Define 3D NAND Memory Array

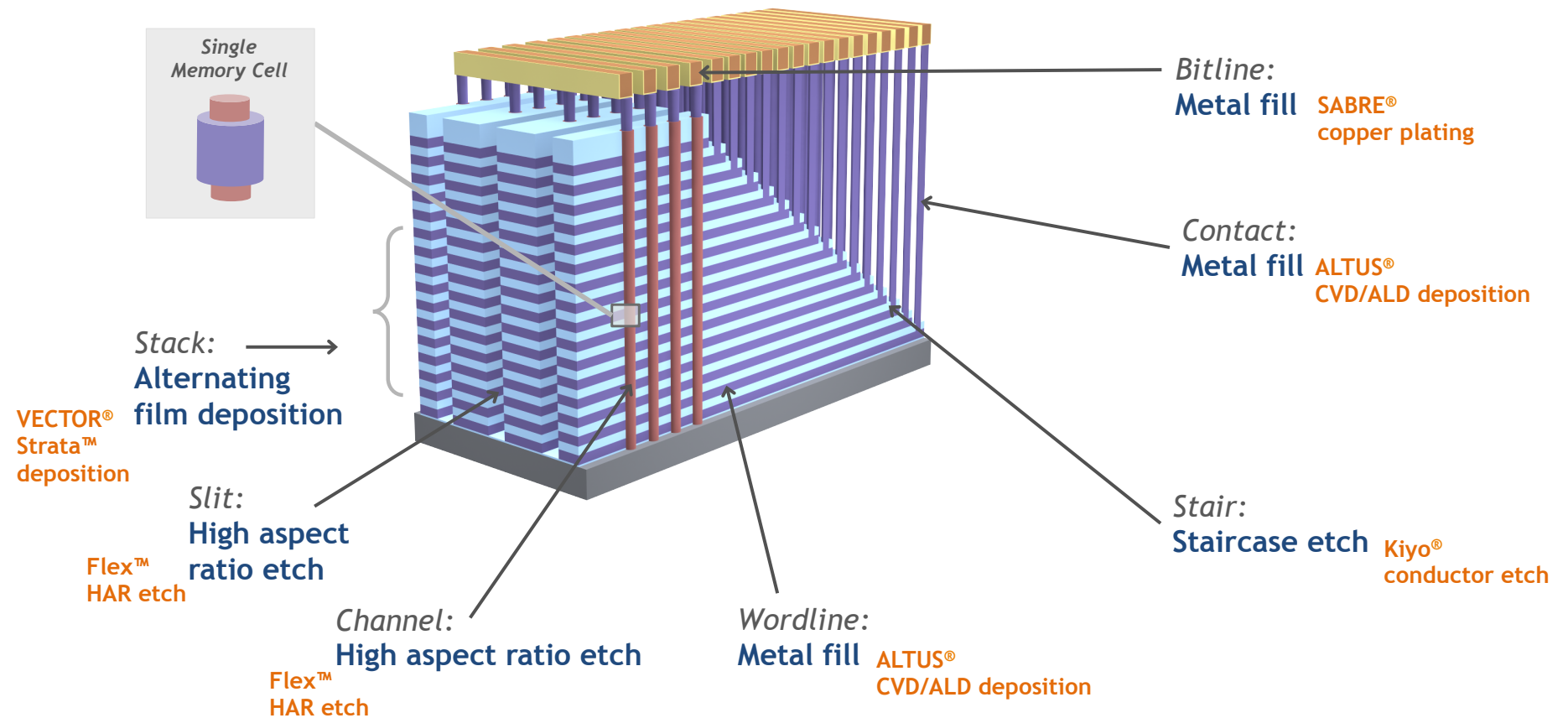


Deposition and Etch Processes Define 3D NAND Memory Array

Deposition and Etch Processes Define 3D NAND Memory Array



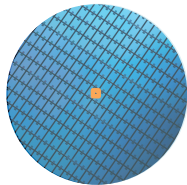
Deposition and Etch Processes Define 3D NAND Memory Array



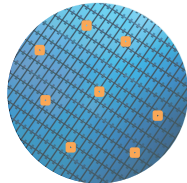
3D NAND Etch Process Challenges: Lam Etch Solutions

Etch Challenges

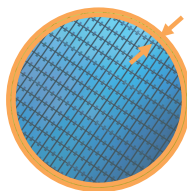
Within-Die



Across Wafer

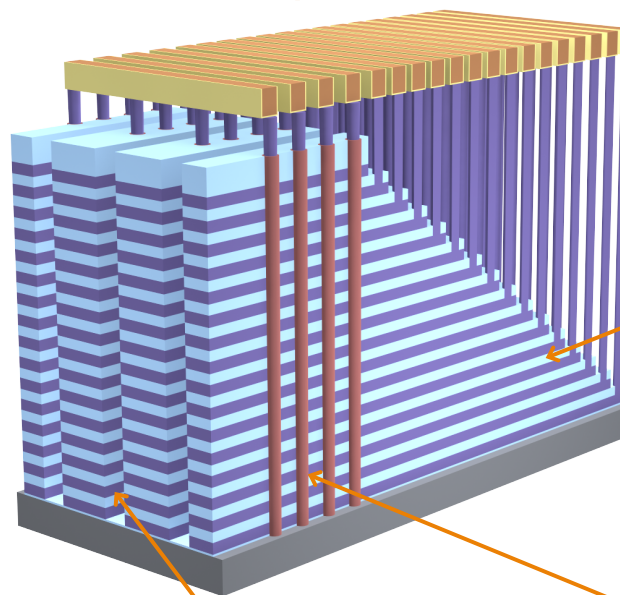


Wafer Edge



Lam Solutions

#1 in deposition and etch markets served



Multi Level Contact:
High aspect ratio etch

Flex™ dielectric etch

Stair:
Staircase etch

Kiyo® conductor etch

Slit:
High aspect ratio etch

Flex™ dielectric etch

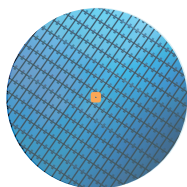
Channel:
High aspect ratio etch

Flex™ dielectric etch

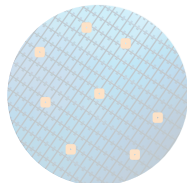
3D NAND Etch Process Challenges: Etching High Aspect Ratios

Etch Challenges

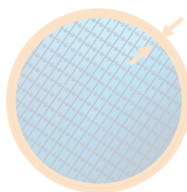
Within-Die



Across Wafer



Wafer Edge

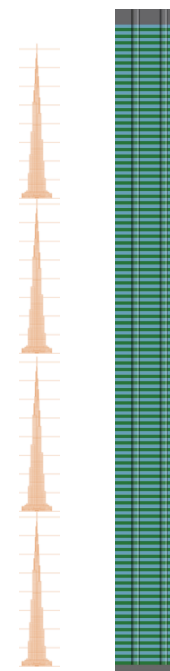


Aspect Ratio = 9:1



The Burj Khalifa, tallest structure in the world

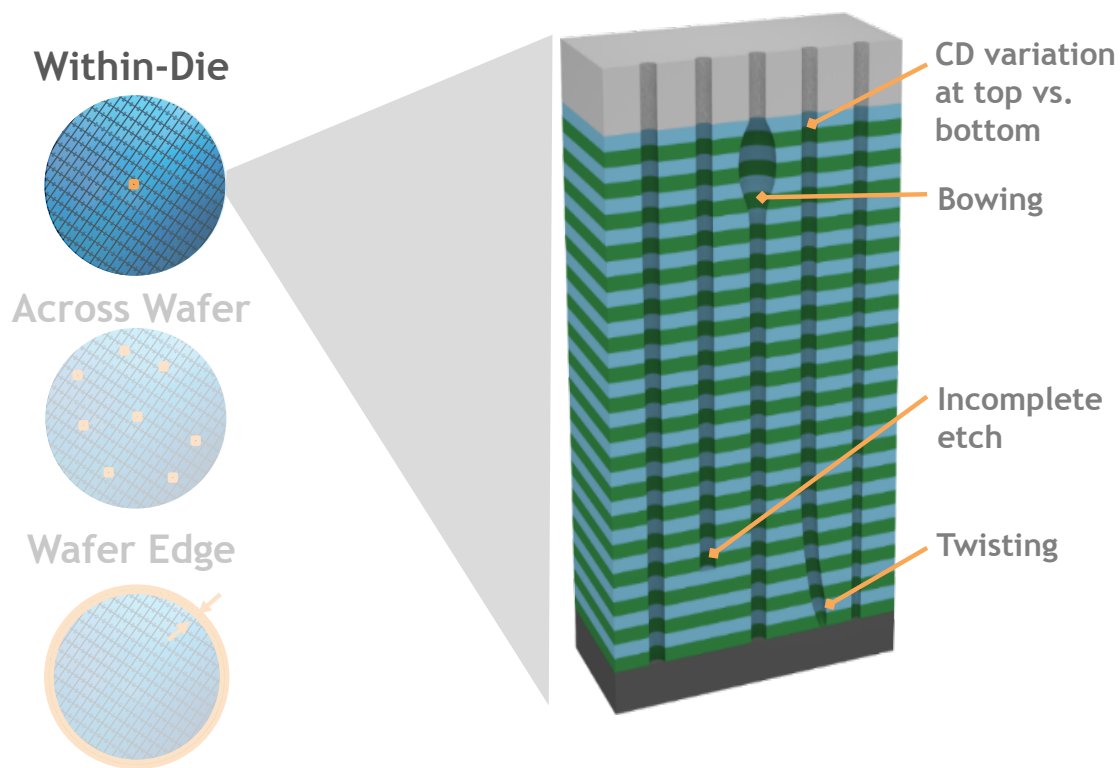
Aspect Ratio = >40:1



Channel hole etched for 90+ layer 3D NAND

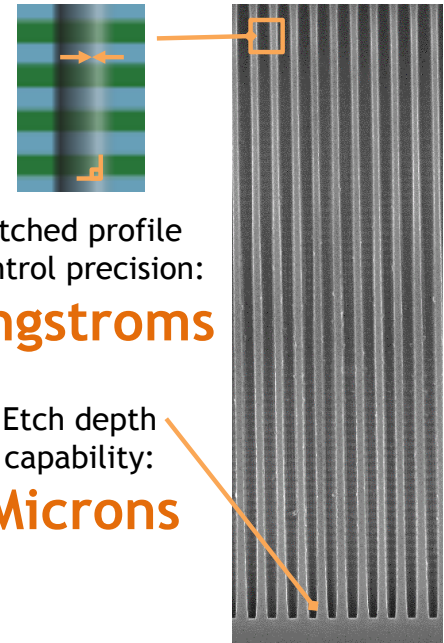
3D NAND Etch Process Challenges: Etching High Aspect Ratios

Etch Challenges



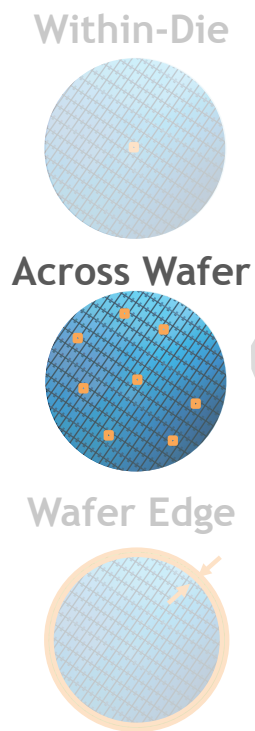
Flex™ channel hole etch

Atomic-scale process control is required in addition to micron-scale etched depths



3D NAND Etch Process Challenges: Uniform Etch Across the Wafer

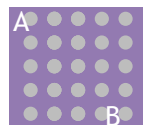
Etch Challenges



Channel holes etched
> 1 trillion per wafer

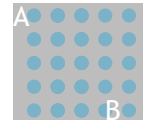
Manufacturing sequence:

1. Post litho



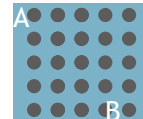
CD A \neq CD B
CD variation

2. Hardmask etch



CD A = CD B
CD uniformity improved

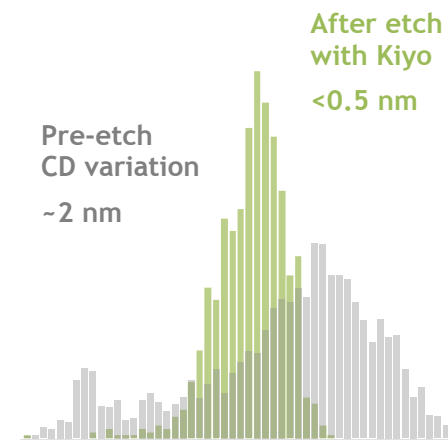
3. Channel hole etch



CD A = CD B
Uniform CD transferred

Kiyo[®] patterning etch

Mask open patterning fidelity
improves channel uniformity



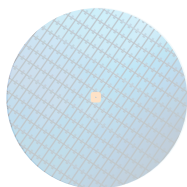
Distribution of CDs after etch

5 Å, 3 σ

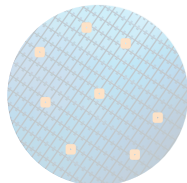
3D NAND Etch Process Challenges: Extreme Edge Control of Yield

Etch Challenges

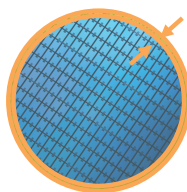
Within-Die



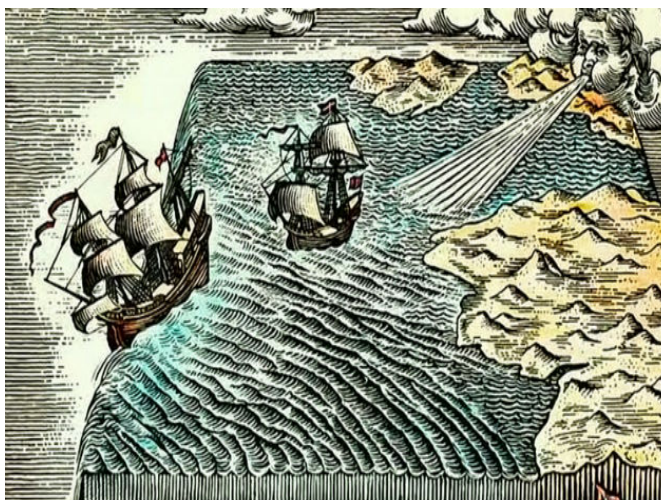
Across Wafer



Wafer Edge

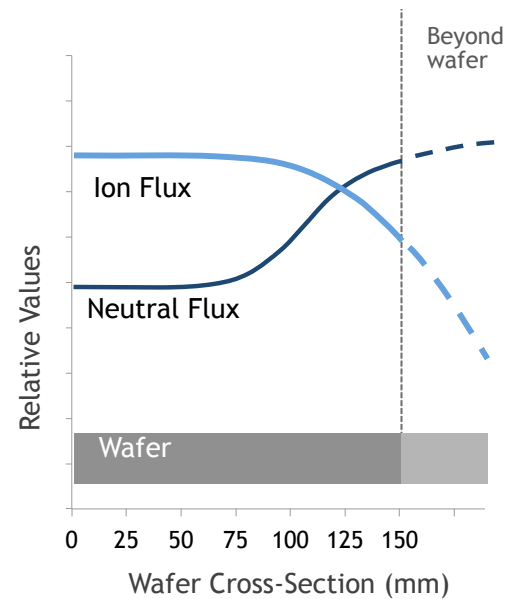


Strange things happen at the edge of the wafer



Outer 8 mm of wafer:
~10% of die

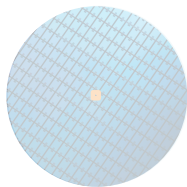
Finite wafer size creates gradients in fluxes of ions and neutrals



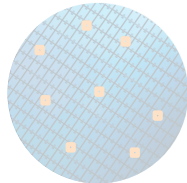
3D NAND Etch Process Challenges: Extreme Edge Control of Yield

Etch Challenges

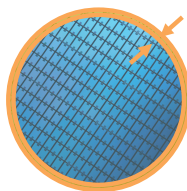
Within-Die



Across Wafer

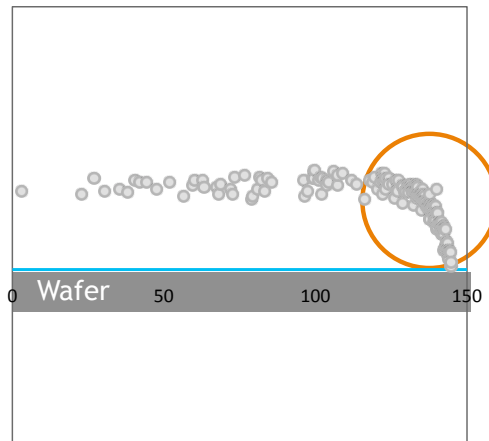


Wafer Edge



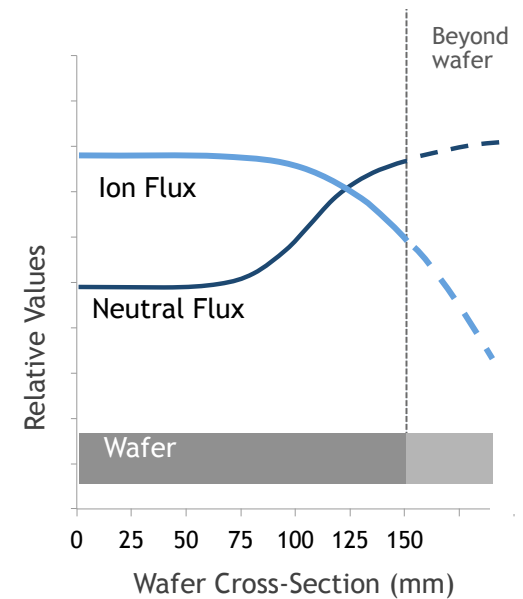
Strange things happen at the edge of the wafer

[CD bias, nm]



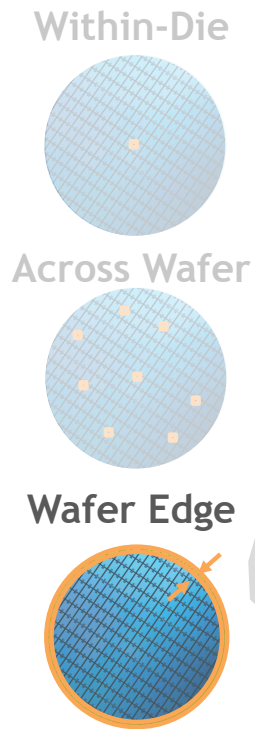
Example: **Non-uniform** CDs at wafer edge

Finite wafer size creates gradients in fluxes of ions and neutrals

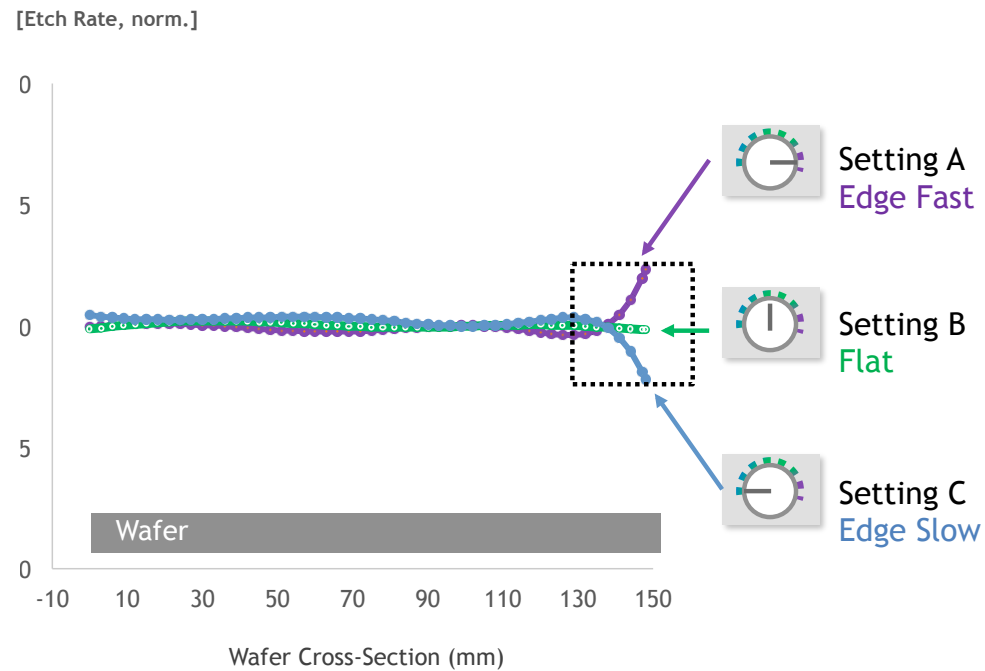


3D NAND Etch Process Challenges: Extreme Edge Control of Yield

Etch Challenges

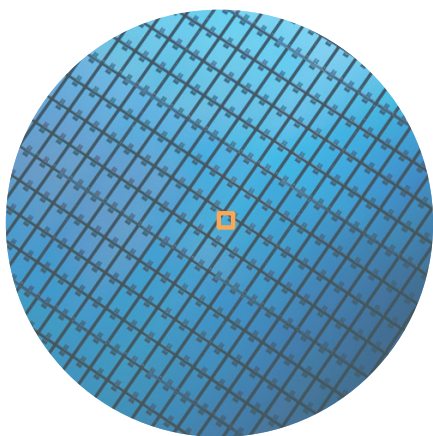


Edge yield can now be optimized during etch:
Corvus™ edge yield control



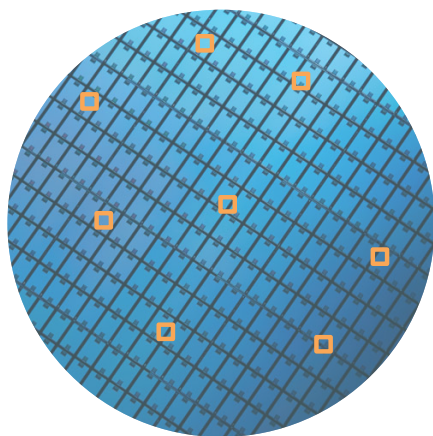
3D NAND Etch Process Challenges and Lam Etch Solutions

Within-Die



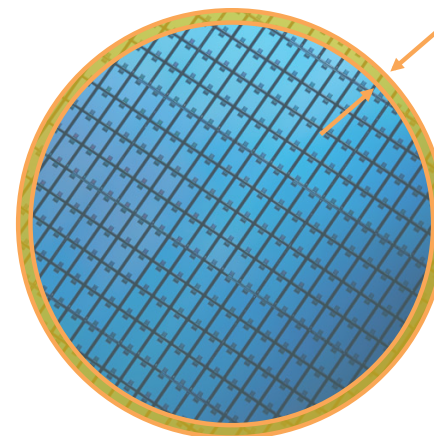
Flex™ high aspect ratio etch
>40:1 etch capability

Across Wafer



Kiyo® patterning capability
5 Å, 3 σ uniformity of CDs

Wafer Edge

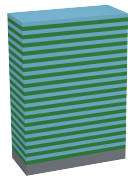


Corvus™ edge yield solution
available on Lam etch
modules

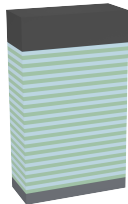
3D NAND Etch Process Challenges: Lam Deposition Solutions

Deposition Challenges

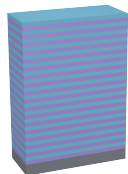
ONON Stack Dep



Hardmask Dep

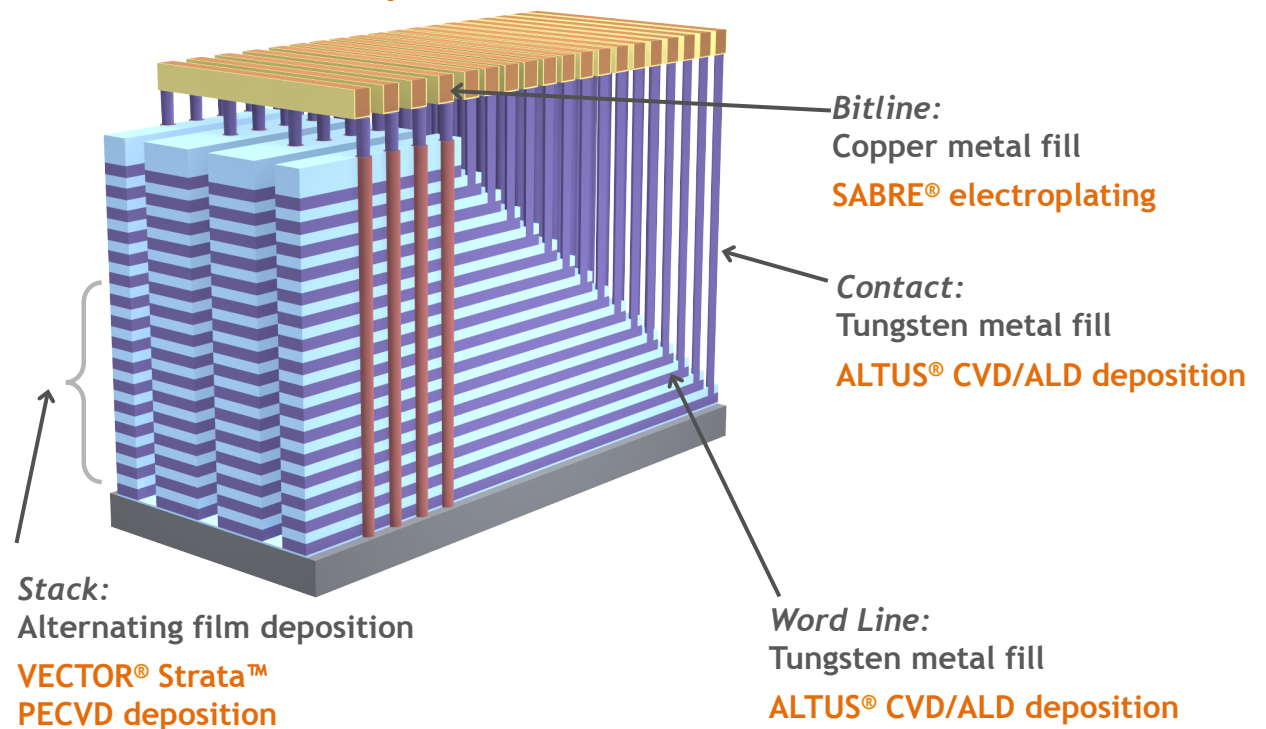


Wordline Fill



Lam Solutions

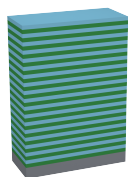
#1 in deposition and etch markets served



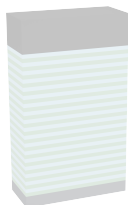
3D NAND ONON Stack Deposition Challenge: Uniform, Low Stress Stack Deposition

Deposition Challenges

ONON Stack Dep



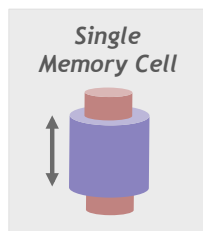
Hardmask Dep



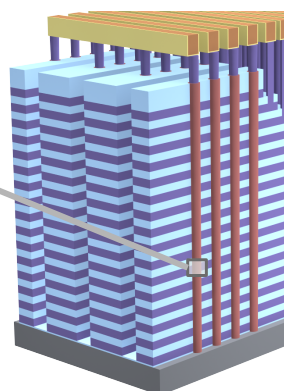
Wordline Fill



Layers deposited
> 200 pairs per stack



N layer thickness
defines the device
gate length



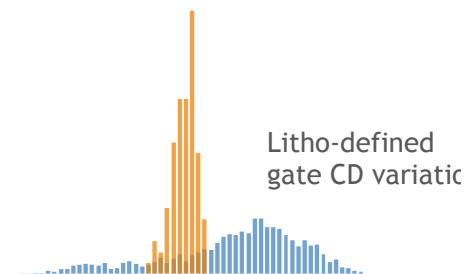
Consistent, uniform film deposition is
critical for patterning accuracy and
electrical performance

VECTOR® Strata™ ONON Stack Deposition

Excellent film thickness control enables
narrower threshold voltage distributions

Uniform ON thickness in
>200 pair stack

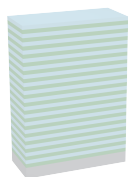
VECTOR Strata N layer
thickness < 0.5nm variation



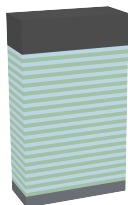
3D NAND Hardmask Deposition Challenge: Mask Selectivity

Deposition Challenges

ONON Stack Dep



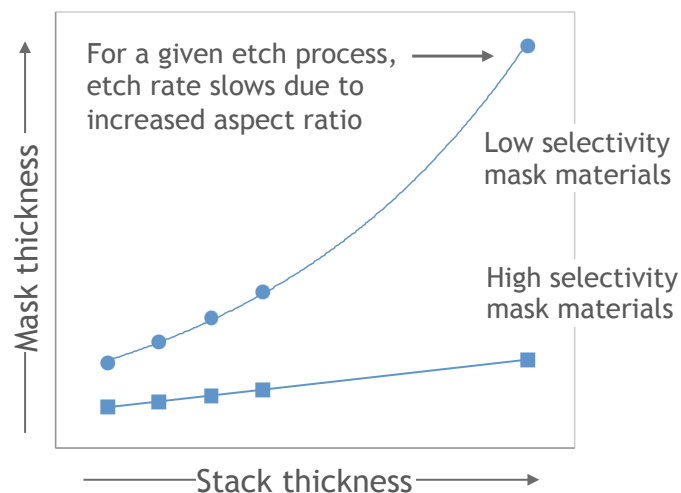
Hardmask Dep



Wordline Fill

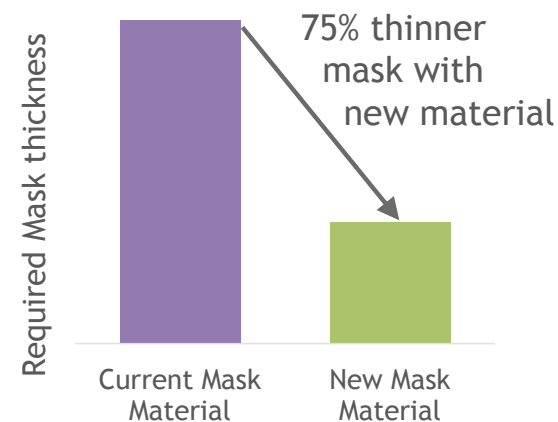


Etch rate slows down with increasing **mask + ONON** thickness



VECTOR® AHM® Hardmask Deposition

New highly selective hardmask material enables thinner mask

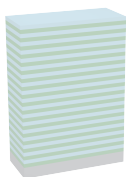


Thinner hardmask enables etch of thicker ONON stack

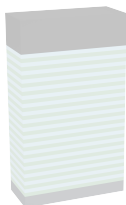
3D NAND Wordline Fill Challenge: Moving Reactants In and By-Products Out

Deposition Challenges

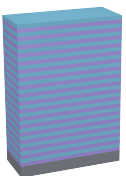
ONON Stack Dep



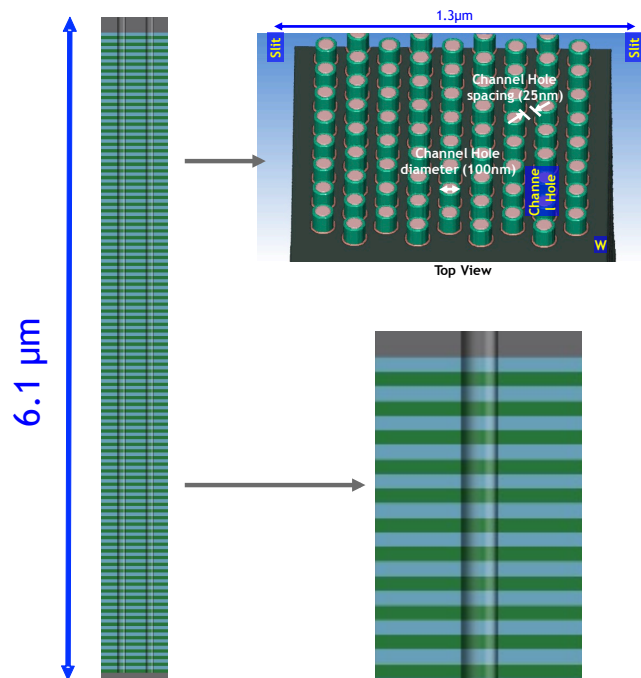
Hardmask Dep



Wordline Fill

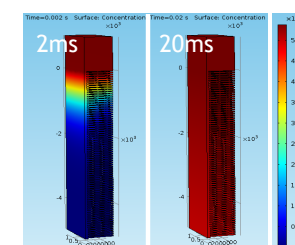


Uniform void-free fill difficult in deep 3D structures



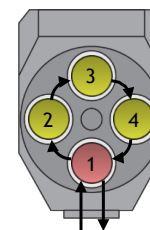
Hardware design changes address these difficulties

Reactant Saturation on Wafer



- Reactant pre-charge volumes increase dose
 - Uniform W deposition top to bottom layer
 - Reduced cycle times

By-Products Removal



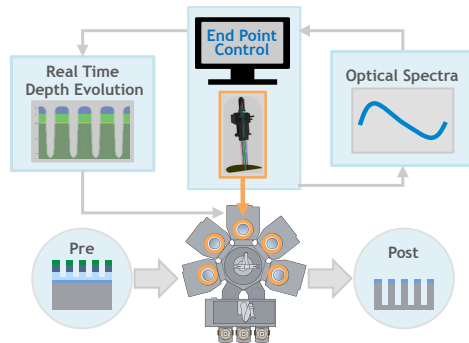
- Combine lower temp nucleation (station 1) and high temp bulk fill (stations 2-4)
 - Reduced F in the film
 - Lower R_s
- Quad-station module (QSM) enables faster temperature transitions
 - Higher productivity

Lam Process Control On-Tool Solutions

Achieve Faster Learning Rate, Reduce Total Cost of Process Control

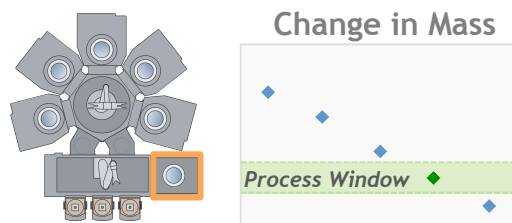
Improved Productivity

- *In situ*, real-time sensors for endpoint control
- Big data analytics for fault detection, drift control and fast matching



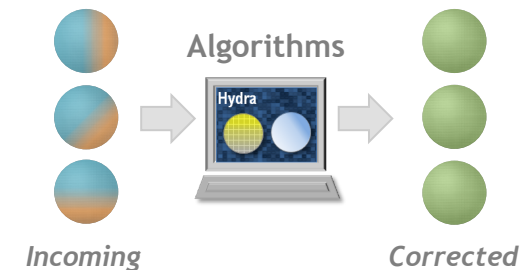
Every Wafer Process Control

- Feedforward and feedback control with integrated metrology
- Customizable APC algorithms
- Virtual metrology



Expanded Process Window

- Litho-etch integrated tuning solutions for CD and overlay
- Computational models enable improved process window



Lam expanding capability with collaborations and continued investment

Summary

3D NAND manufacturing is deposition and etch intensive

Increasing number of layers present unique challenges in delivering high aspect ratio structures with atomic scale process control

Various options examined to extend 3D NAND roadmap to achieve higher bit density and lower cost

Solutions presented for:

- Uniform high aspect ratio etch with extreme edge control of yield
- Low stress stack depositions, mask selectivity, and wordline fill



Innovative **Technology**
Trusted **Productivity**
Fast **Solutions**

