Flash Memory Summit

Overcoming Higher Bit Error Rates in New NAND Technologies

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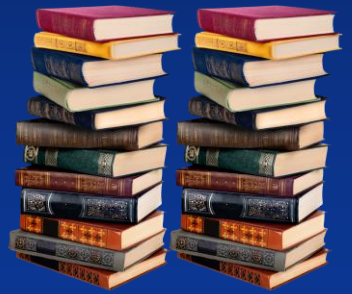
SSD & NAND

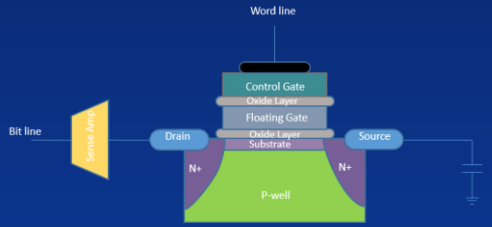


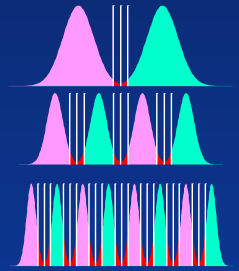
The increasing BER

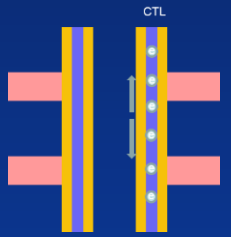
Feature size shrinks

Quantization level doubles

3-D layer grows

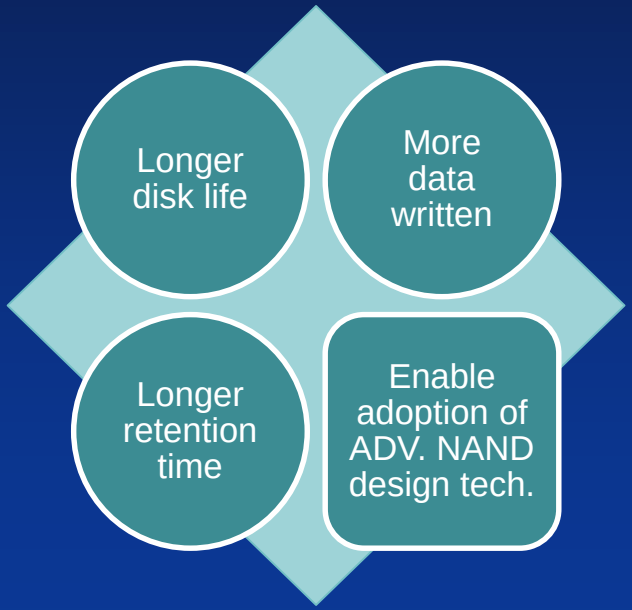






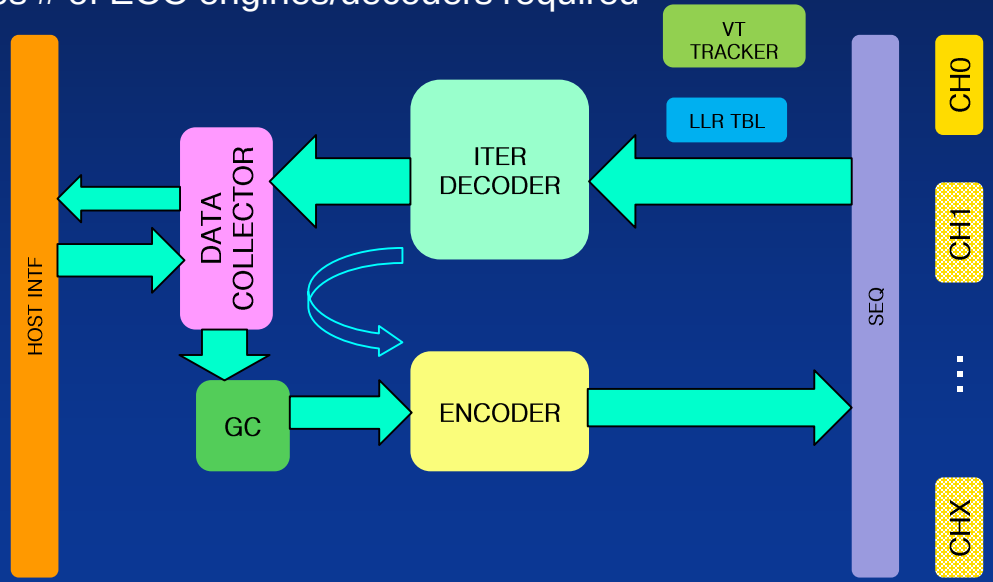
Role of ECC

- Provide more value to customer



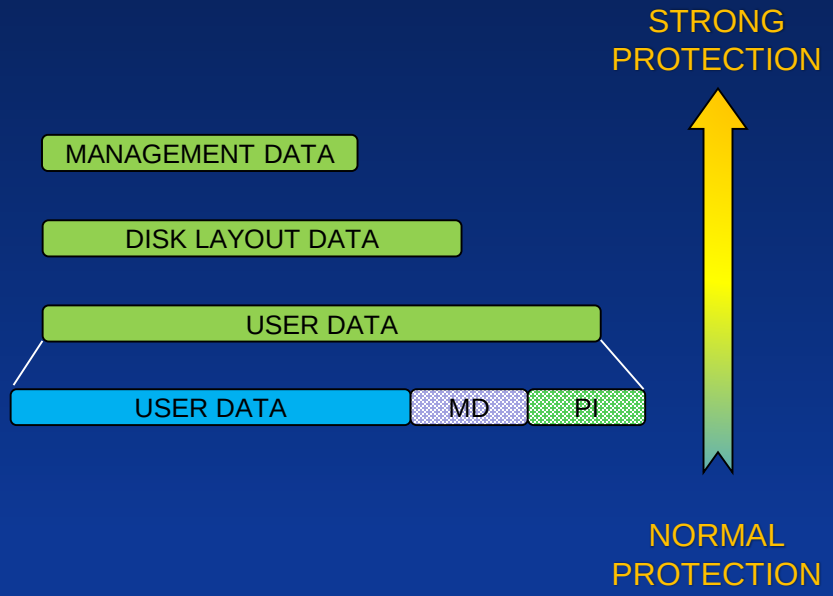
ECC Evaluation: Throughput

- ECC Throughput
  - Impact the bandwidth of the system
  - Determines # of ECC engines/decoders required



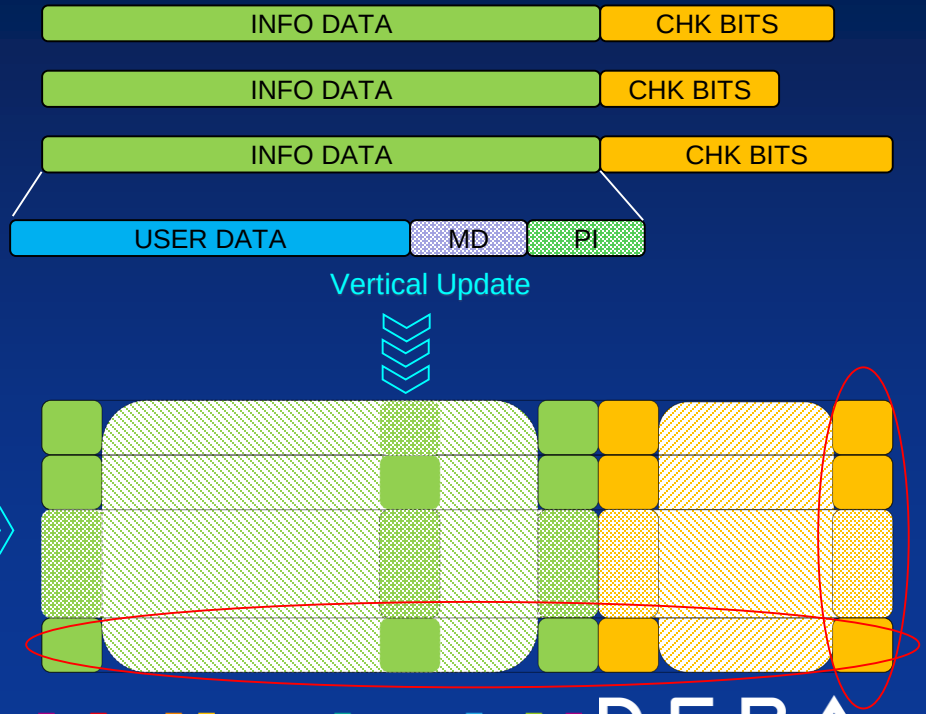
ECC Evaluation: Flexibility

- Flexibility
  - Multiple code rate: different data types are stored in different region/field
  - Variable metadata/application data



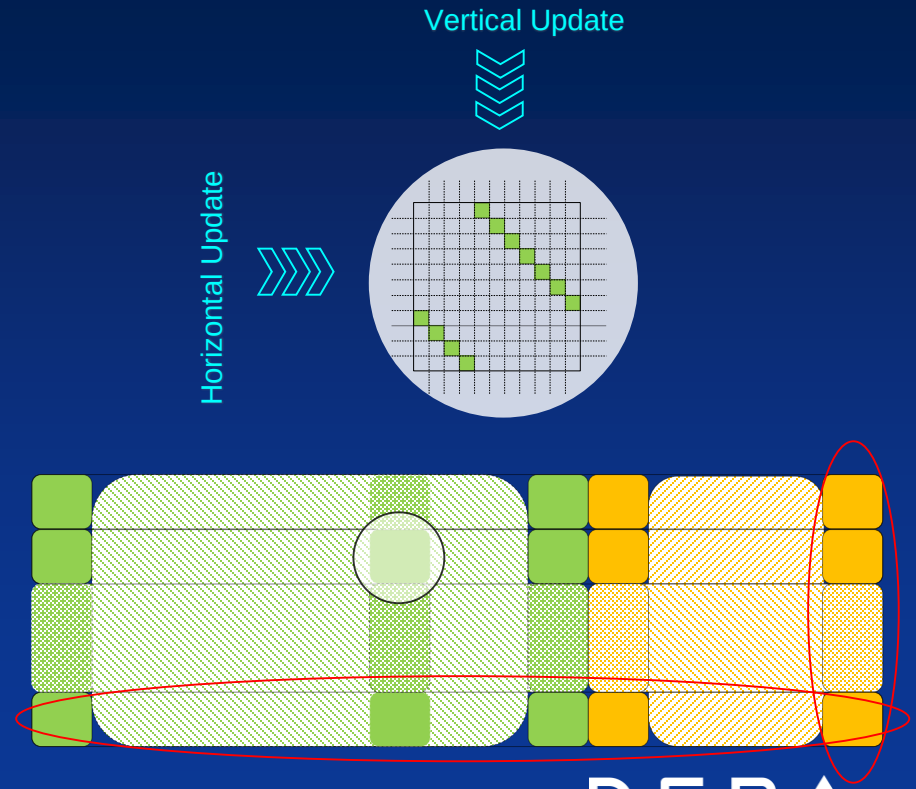
Flexibility(Cont'd) & Impact on design

- Parameter & Structure
  - Identity matrix size – multi-coderate & performance
  - Data rescue methods



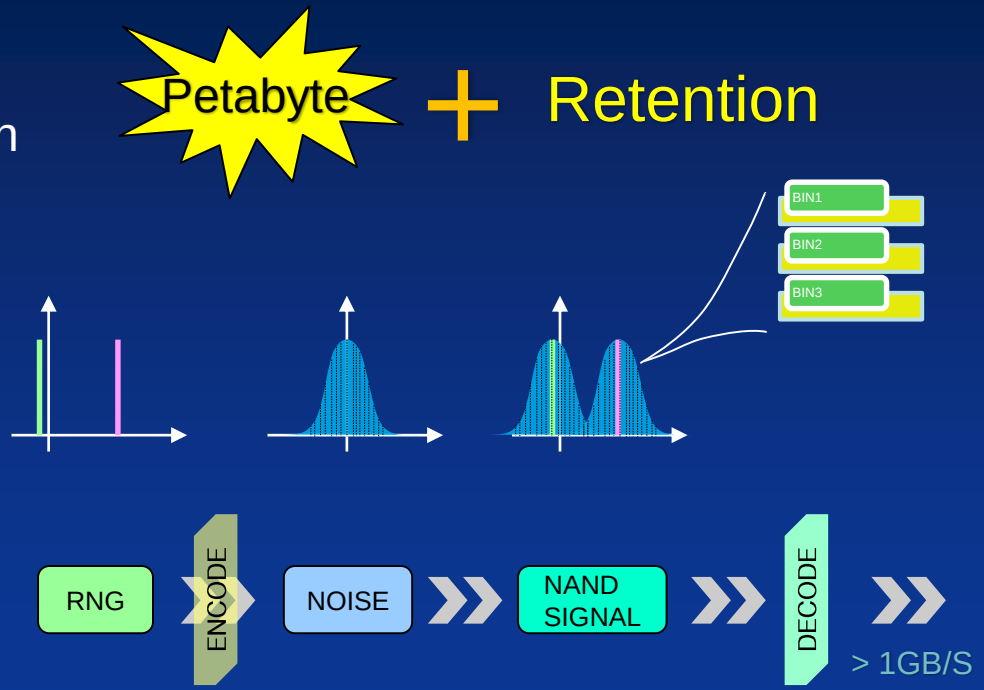
Implementation complexity

- Case study of hardware limitation
  - SOC design limitation – layered shuffling & soft constraint
  - FPGA prototyping – info compression engine



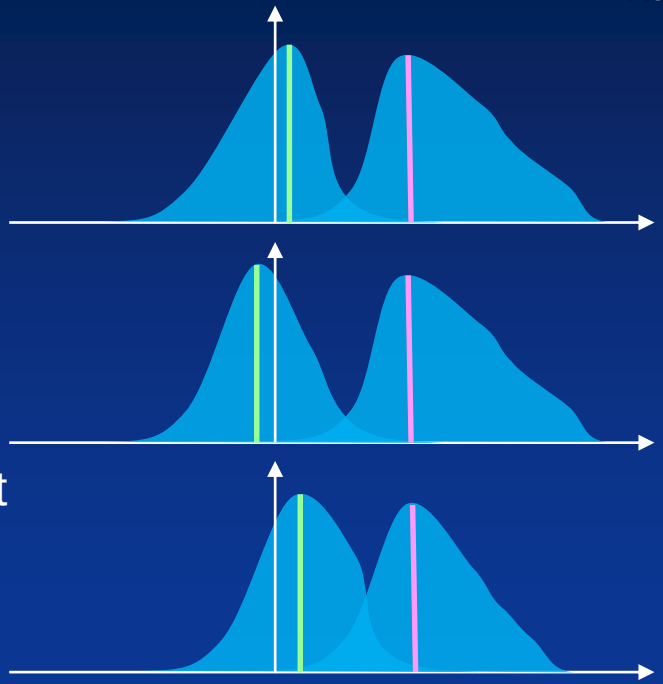
Accelerated simulation

- Accelerated simulation
  - NAND signal emulation – high speed & high precision
  - LLR generation – vt placement



Stimulus Generation

- NAND-Char & Accelerated simulation
  - Life time NAND characterization – classification: curve parameters
  - Correlate NAND-Char result with Noise distribution – generation policy



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Thank you!

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