Two-Level Code Construction Using LDPC Codes

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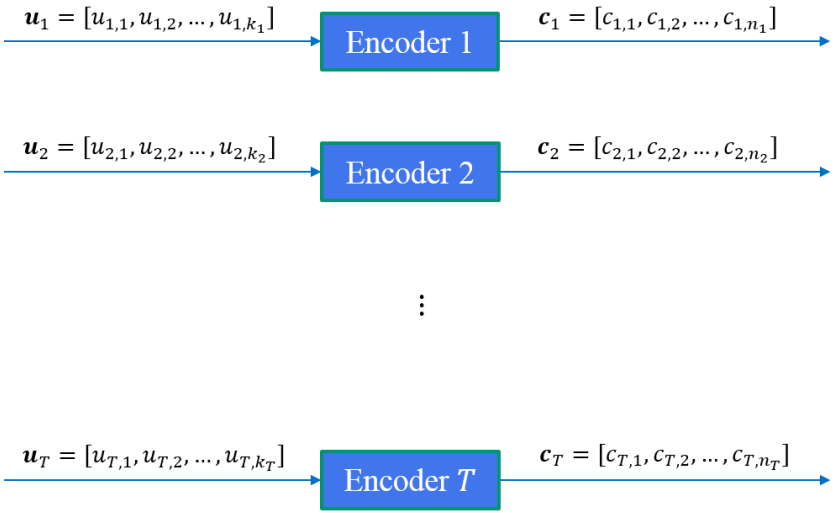
Overview

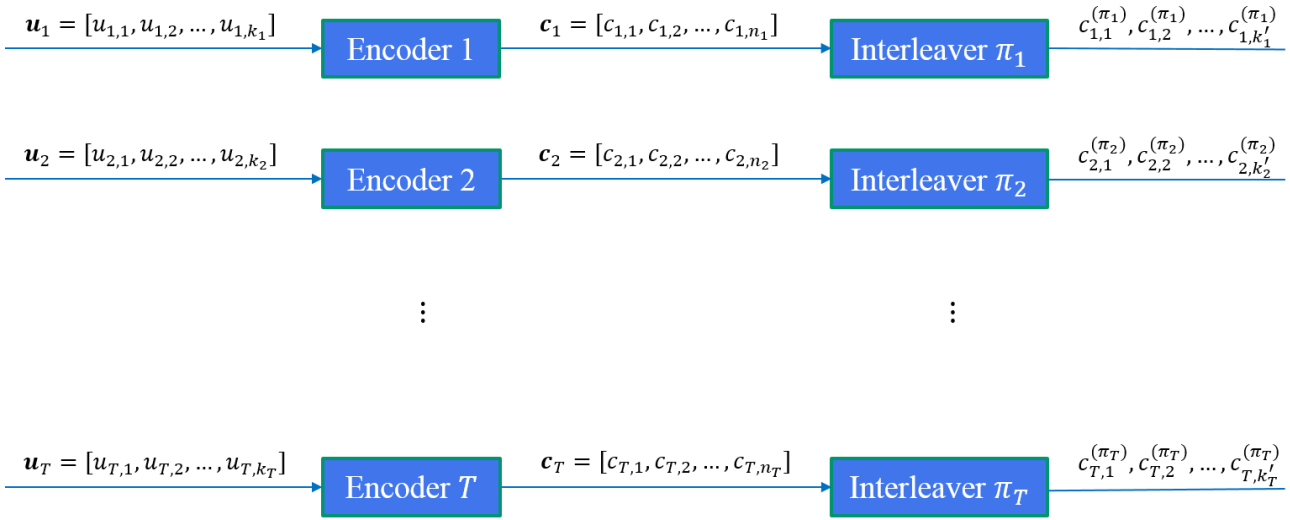
- Encoding
- Decoding
- Memory Requirements
- Latency
- Simulation Results
- Summary

Encoding



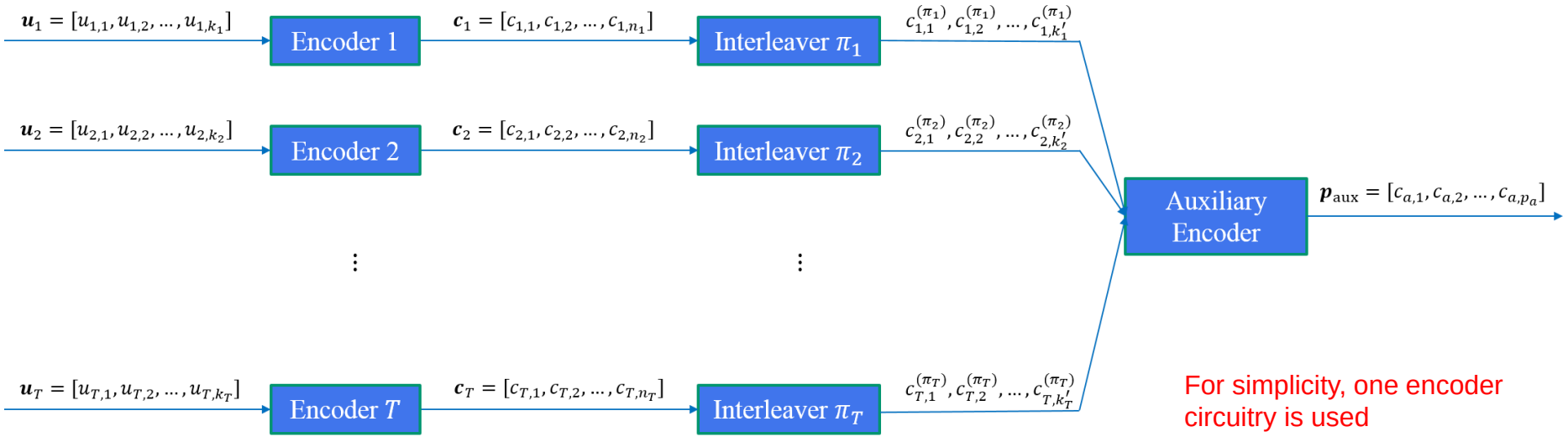
T is the page size

Encoding



T is the page size

Encoding

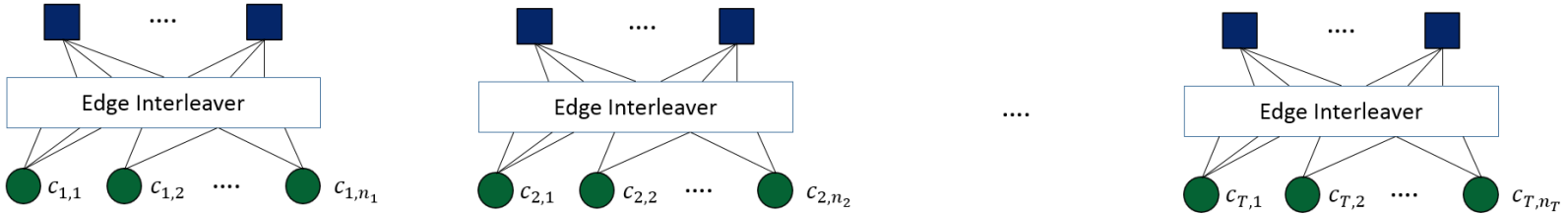


T is the page size

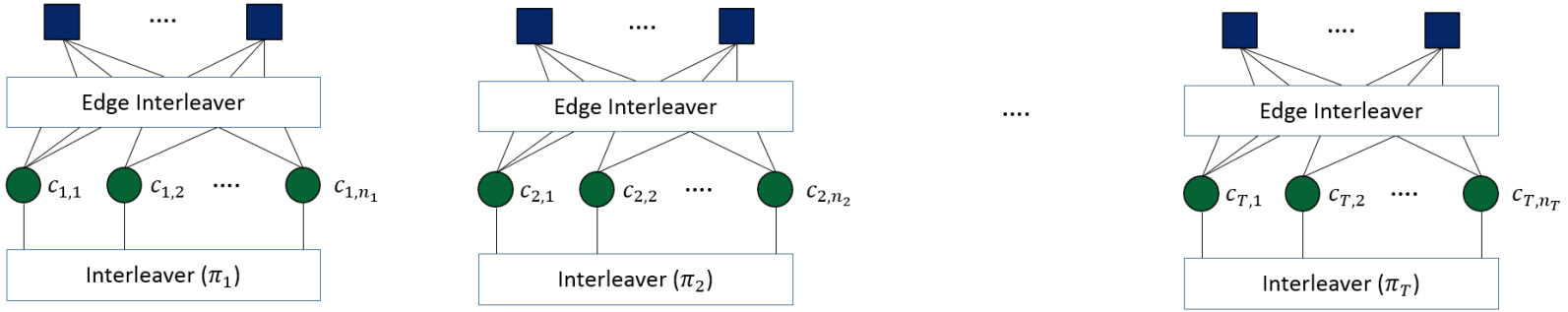
For simplicity, one encoder circuitry is used

Only $\boldsymbol{p}_{\text{aux}}$ is stored

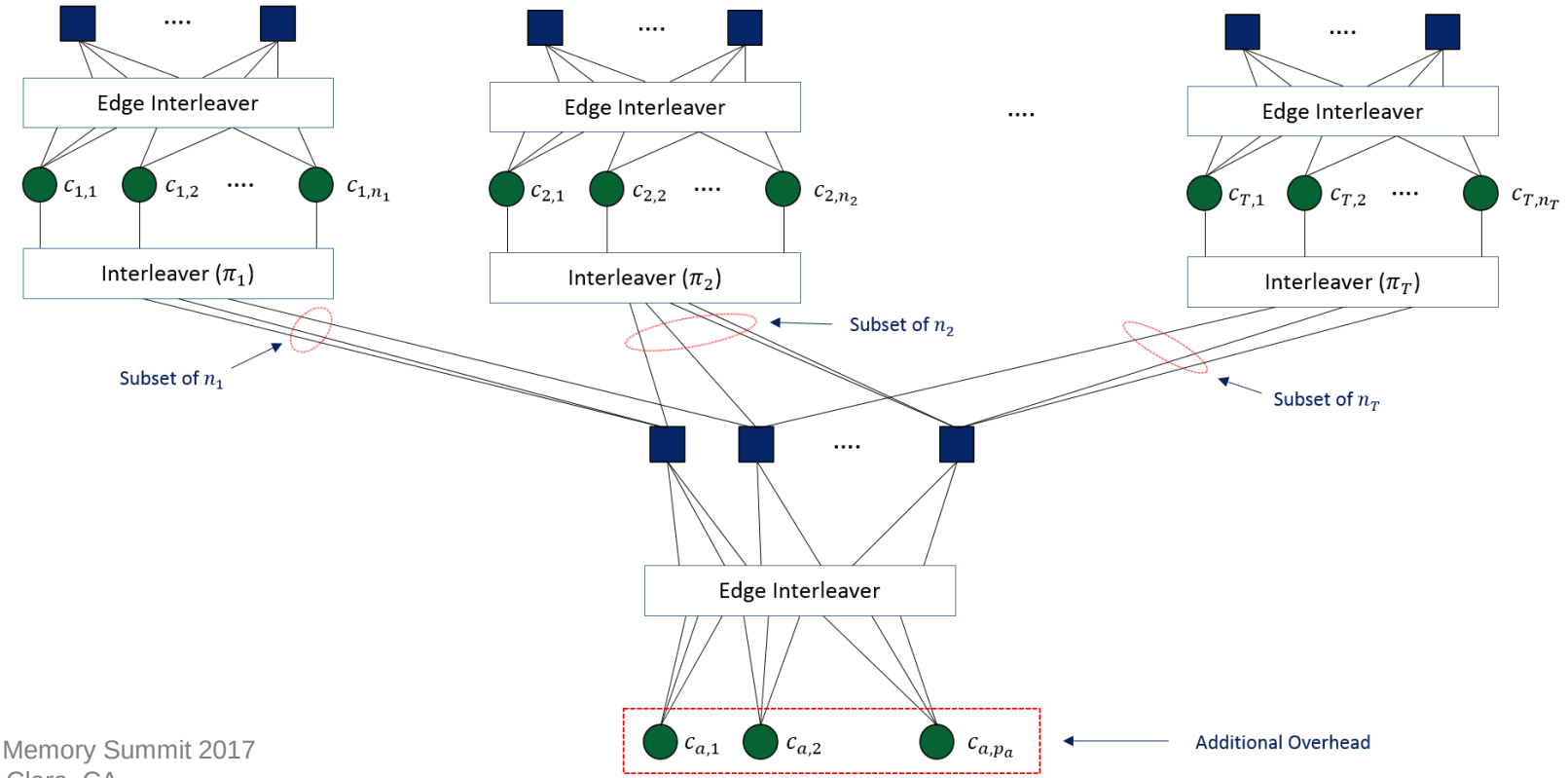
The Code Graph



The Code Graph



The Code Graph



Decoding

Step 1. Decode the T primary codewords in one memory page

d_f: number of decoding failures

If $d_f = 0$,

decode the T primary codewords in the next page;

else

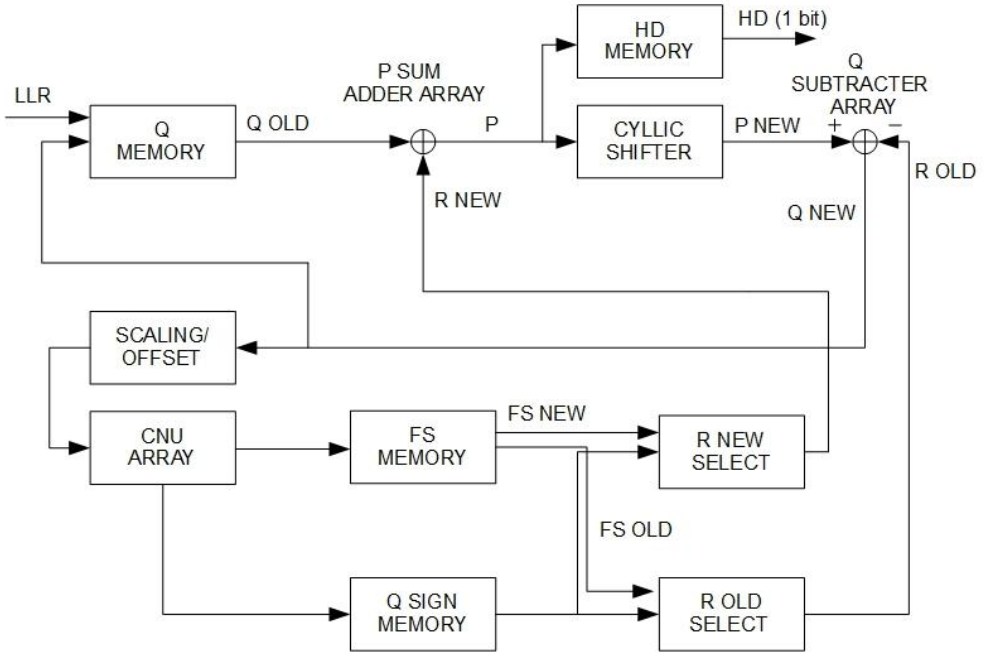
for $m = 1, \ldots, d_f$

Step 2. If the auxiliary codeword has not been decoded yet, compute its LLRs and decode it.

Step 3. Update the LLRs of the failed primary codeword based on the results of Step 2 and decode it one more time.

Memory Requirements: One-Level Code

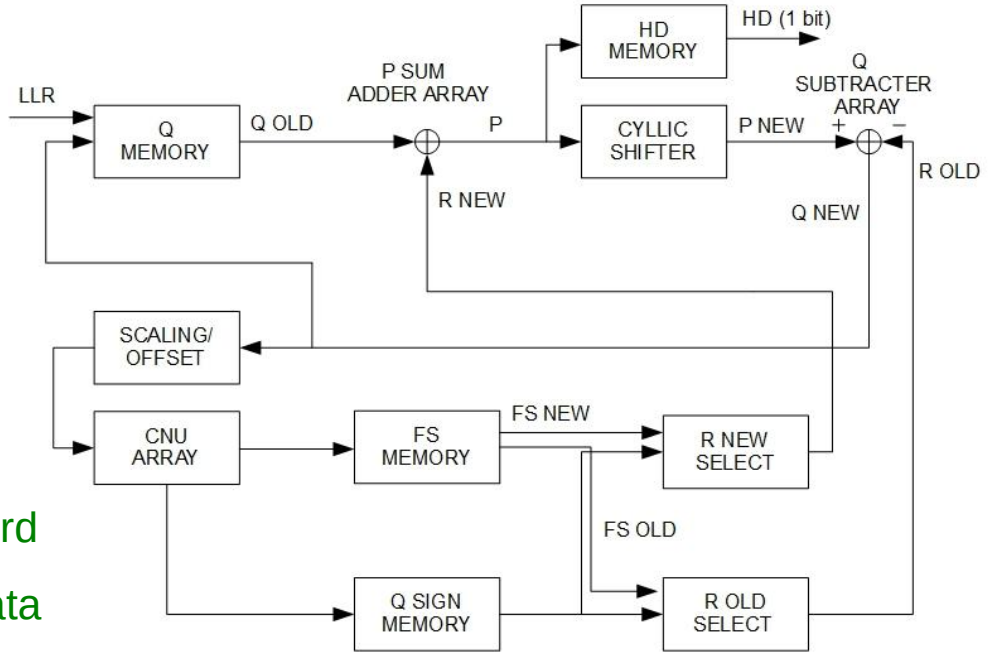
- Double buffered Q memory
- Double buffered HD memory
- Qsign memory
- FS memory



The block serial layered decoder
(the most memory efficient decoder architecture)

Memory Requirements: Two-Level Code

- Only one decoder circuit used
- Double buffered Q memory
- Double buffered HD memory
- Qsign memory
- FS memory
- HD memory for the failed codeword
- ROM to store the connectivity data of the auxiliary and primary codes



The block serial layered decoder
(the most memory efficient decoder architecture)

Latency

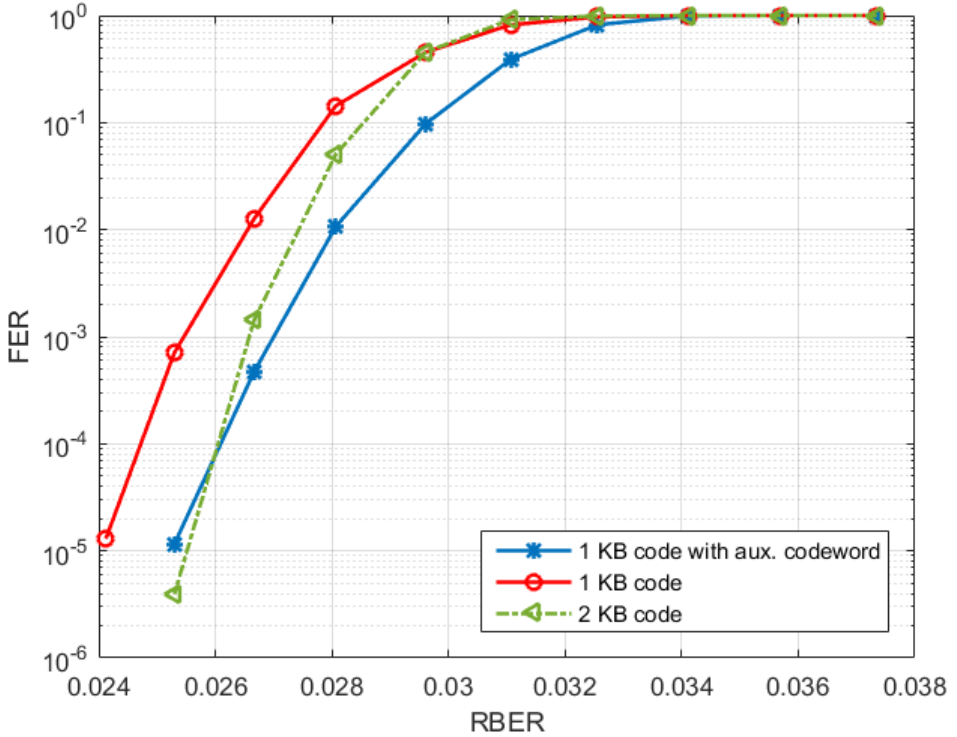
- Latency introduced only when the auxiliary codeword utilized
- Sources of latency:
  - Load the HDs related to the last primary codeword in the auxiliary codeword's HD memory (bc : block columns)
  - Read the parity bits of the auxiliary codeword (p : parity blocks)
  - Decode the auxiliary codeword (decoding algorithm, parallelization)
  - Load the HD detection results of the failed codeword for decoding (bc)
  - Decode the failed codeword one more time (decoding algorithm, parallelization)

Example

- FER = 10^{-4} : 1 out of 10000 packets fails on the average
- Rate = 0.91, block columns = 66, parity blocks = 6, non-zero circulants = 264
- Parallelization = circulant size, Page size = 16, Average iterations = 3
  - Load the HDs of the last primary codeword: 66 clks
  - Read the parity bits of the auxiliary codeword: 6 clks
  - Decode the auxiliary codeword: 3 x 264 = 792 clks
  - Load the HD detection results of the failed codeword: 66 clks
  - Decode the failed codeword one more time: 792 clks
  - Overall page latency = 1722 / (16 × 792) = 13.6% (for 0.01% of the packets)
  - For 99.99% of the packets, the latency same as the one-level system

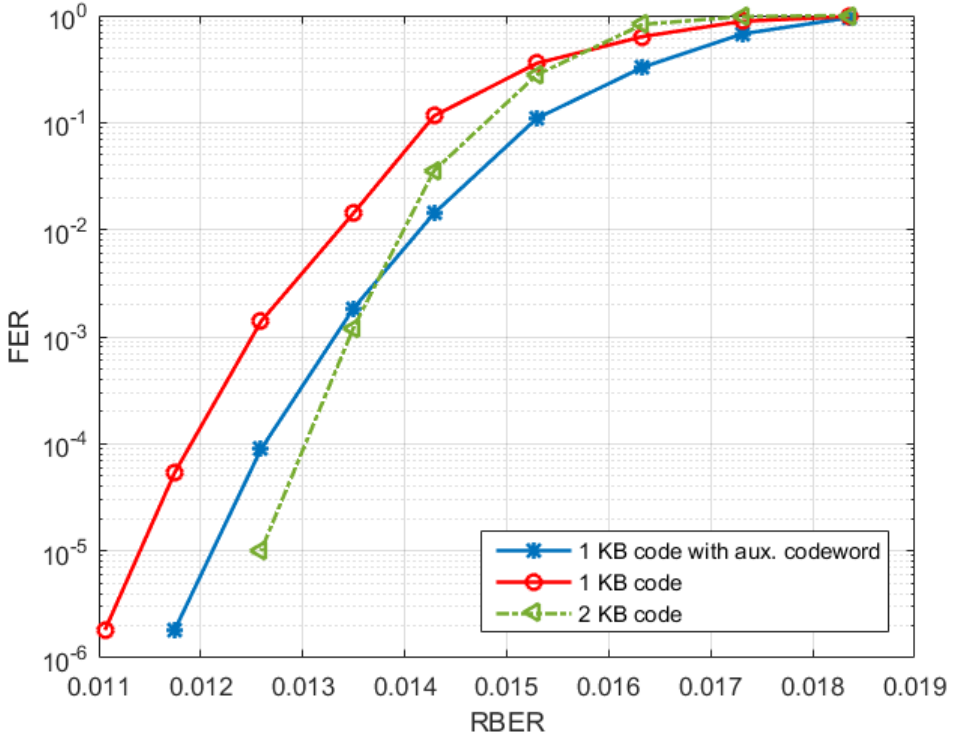
Simulation Results (1)

- Rate = 0.83
- Length = 1 KB
- T = 16
- Circulant size = 140
- Binary LDPC codes



Simulation Results (2)

- Rate = 0.91
- Length = 1 KB
- T = 16
- Circulant size = 140
- Binary LDPC codes



Summary

- A two-level code construction scheme based on LDPC codes presented
- Improved frame error rate (FER) performance compared to one-level scheme
- Small memory requirements, particularly, when utilized with memory efficient architectures
- Negligible latency at low FER regime

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Thank You!