ECC Approach for Correcting Errors Not Handled by RAID Recovery

Jeff Yang
Siliconmotion

Note: All the material are the concept proof and simulation. It is not the real Siliconmotion’s final product.
Traditional Error recovery flow

Error recovery flow

- Hard decoding
- Moving Read (Using read-retry table)
- Soft-decoding (Iterative decoding)
- Noise Cancellation
- RAID protection (addition parity)
- DISK Rescue

- High efficiency
- High complexity
- Strong correction capability
- Lower trigger rate

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3D NAND Challenges

- Each 3D generation will increase the layer number by 30~50%.
- High-aspect ratio channel hole etch.
- Cell current reduction is seriously concerned.
- Reduce the read-voltage to improve the read-count (degradation the read-disturbance) make cell current worse.
- Different cell characteristics for each WL. (program-speed, cell-to-cell interference, retention)
- Poor retention characteristics.

Not easy to screen out some defects
Especially on bit-column related defect.
RAID is good, but….

- Put the data from the same failure range into the different RAID protection group.
- Add more write overhead, because the additional parity will be written.
- If the failure range cross the block, a plan based protection range is needed.

12.5% overhead

50% overhead in single chip applications
A read back verify scheme

- The SLC to TLC internal copy will be used to accelerate the write performance and power saving. (cause some random error bit.)
- If the TLC write complete, there is still a probability on TLC read fail from read-disturbance, X-temp, or Data-retention.
Bit column related Failure

Fail Position Chunk Index0

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Bit column related Failure (Zoom-in)
Column fail after Low P/E cycle
Column fail after median P/E cycle
Column fail after high P/E cycle
Vth plot after the P/E cycle

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Erase Vth plot after the P/E cycle

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PV1 Vth plot after the P/E cycle
PV2 Vth plot after the P/E cycle
PV3 Vth plot after the P/E cycle
PV4 Vth plot after the P/E cycle

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PV5 Vth plot after the P/E cycle
PV6 Vth plot after the P/E cycle
Soft-decoding vs. HRE

- These strong error (high reliability error, HRE) is grow with the P/E.
- HRE will dominate the LDPC engine’s decoding capability.
- These kinds of HRE is predictable and recordable.
Caching system to record the high frequency HRE location

1. DSP-engine
2. Channel value Buffer 1-sign 2-soft
3. LDPC decoder
4. HRE Identifier
5. If HRE# > threshold
6. Yes
When HRE cause the Decoding fail

1. After the Vth-tracking to get the proper error profile.
2. Decode done, but uncorrectable.
3. Chunk address match.
4. Fix LLR value on the HRE location.
5. Re-decoding.
1KB LDPC simulation result

- The HRE location will be logged.
  - RBER = 1.25% with 50bit HRE: ~99.9% become correctable.
  - RBER = 1.25% with 100bit HRE: ~98% become correctable.
HRE aware iterative decoding

Hard decoding

Moving Read (Using read-retry table)

Soft-decoding (Iterative decoding)

HRE aware iterative decoding

RAID protection (addition parity)

DISK Rescue
Thanks

• Q&A
• Jeff.yang@siliconmotion.com