



Flash Memory Summit

How the emergence of 3D NAND affects Data Recovery and Erasure Verification

Robin England

Senior Research & Development Engineer

Flash Memory Summit 2017
Santa Clara, CA

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SSD Erasure Verification Service (EVS)

Purpose

- Measures and reports on effectiveness of SSD data erasure / sanitization method

Level I (Logical)

- Read LBAs via SSD interface, look for known data pattern

Level II (Physical)

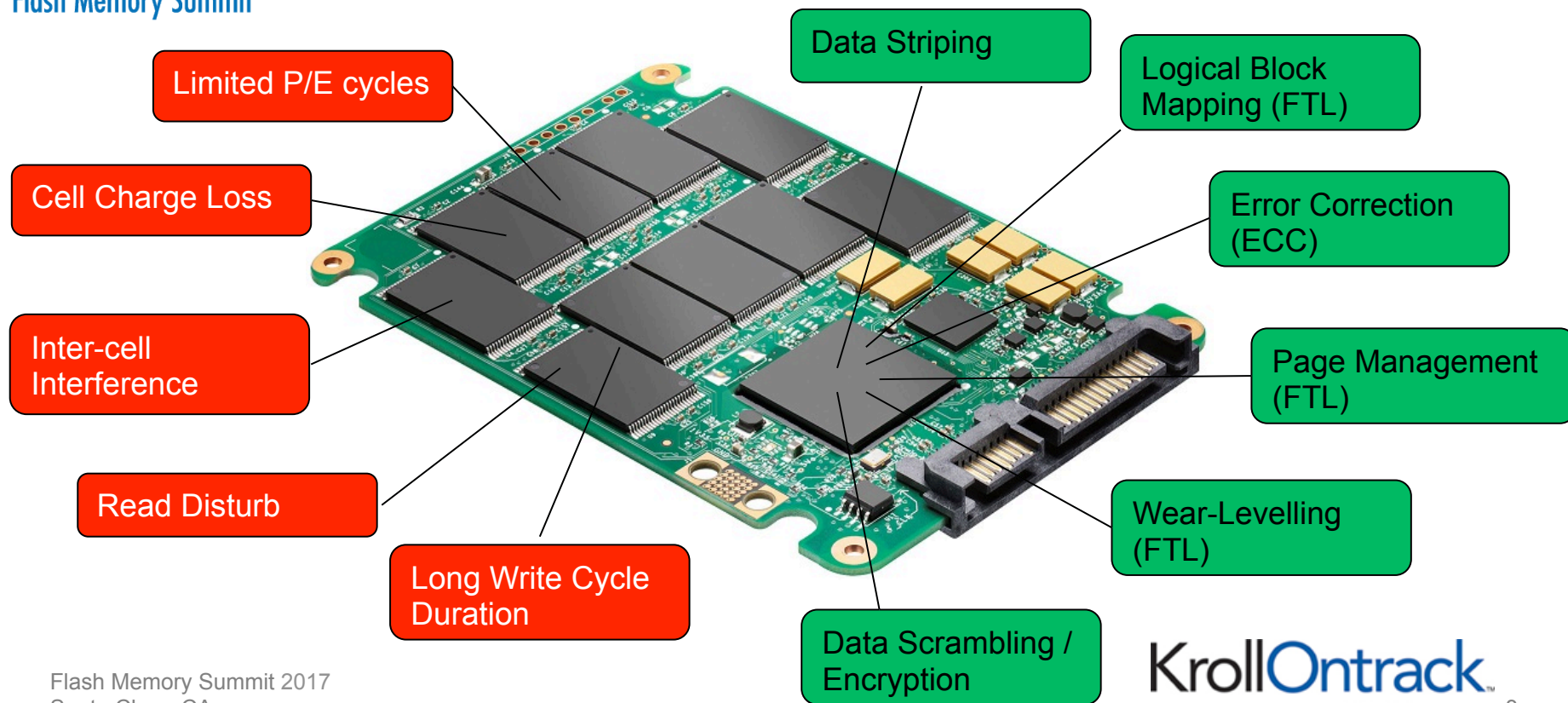
- In-depth examination of SSD NAND flash content, i.e. “Chip-Off” process





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NAND's Challenges & Controller's Solutions



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SSD Chip-Off: EVS versus Data Recovery

Factor	EVS	Data Recovery
Data Striping	✘	✓
Logical Block Map	✘	✓
ECC	~	✓
Page Management	✘	✓
Wear-levelling	✘	✓
Data Scrambling	~	✓
Encryption	~	✓

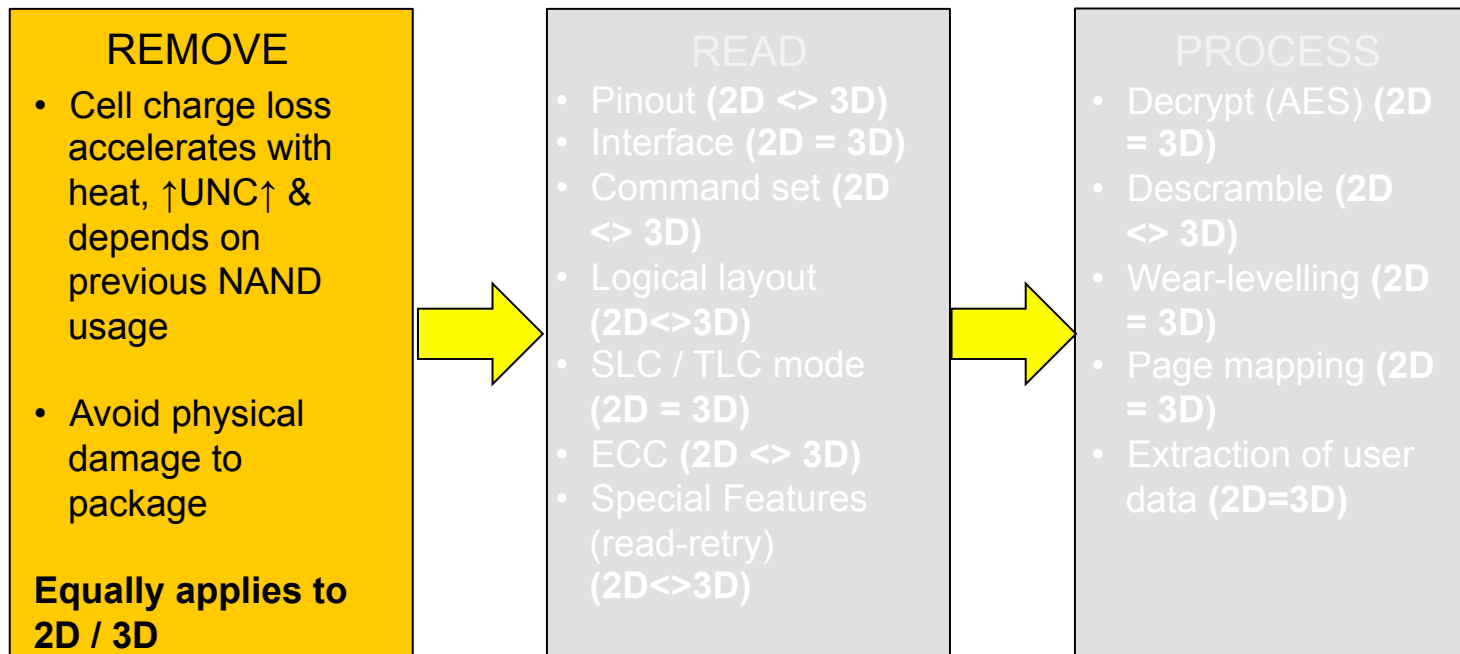
✘ = IRRELEVANT

~ = POSSIBLY

✓ = MUST SOLVE

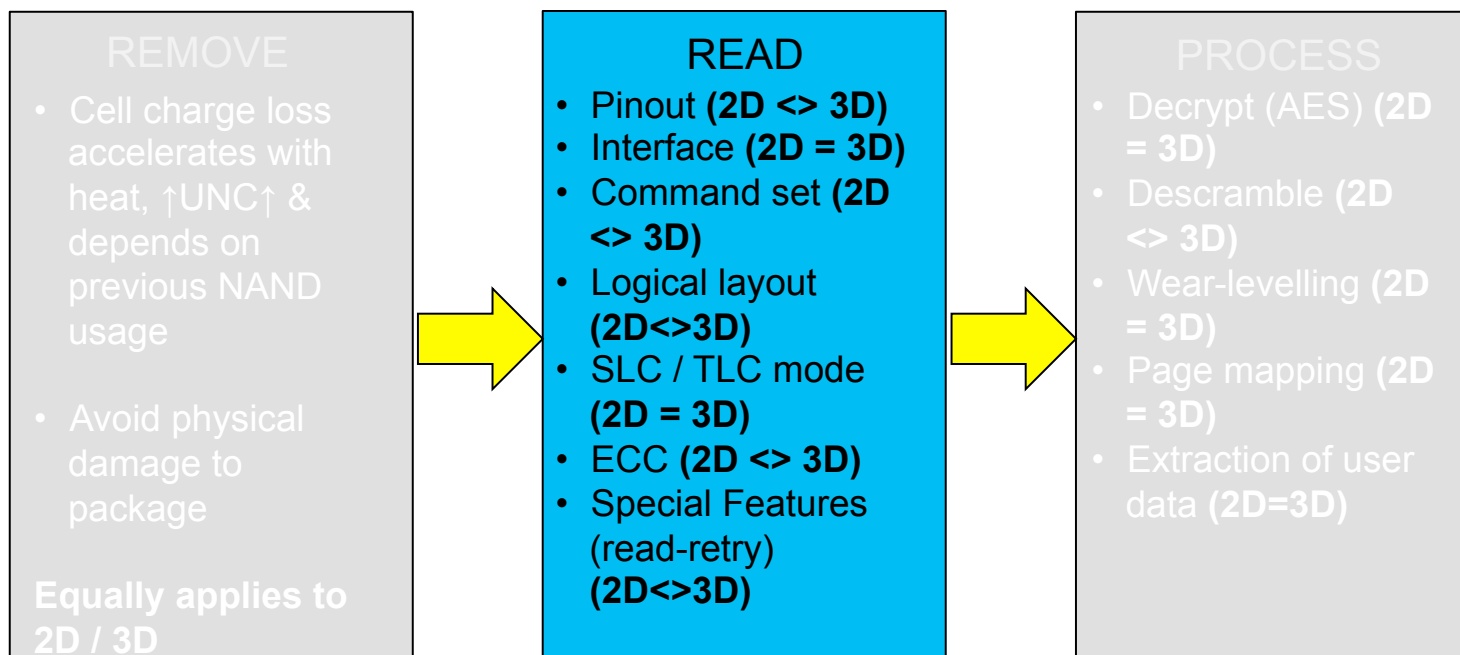


SSD Chip-Off: Remove NAND (2D / 3D)





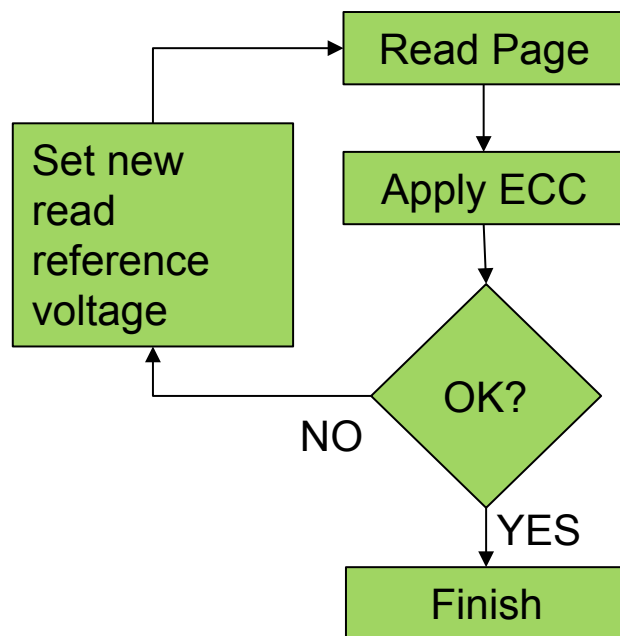
SSD Chip-Off: Read NAND (2D / 3D)





Reading 3D NAND: New Challenges

Read-Retry and ECC cycle

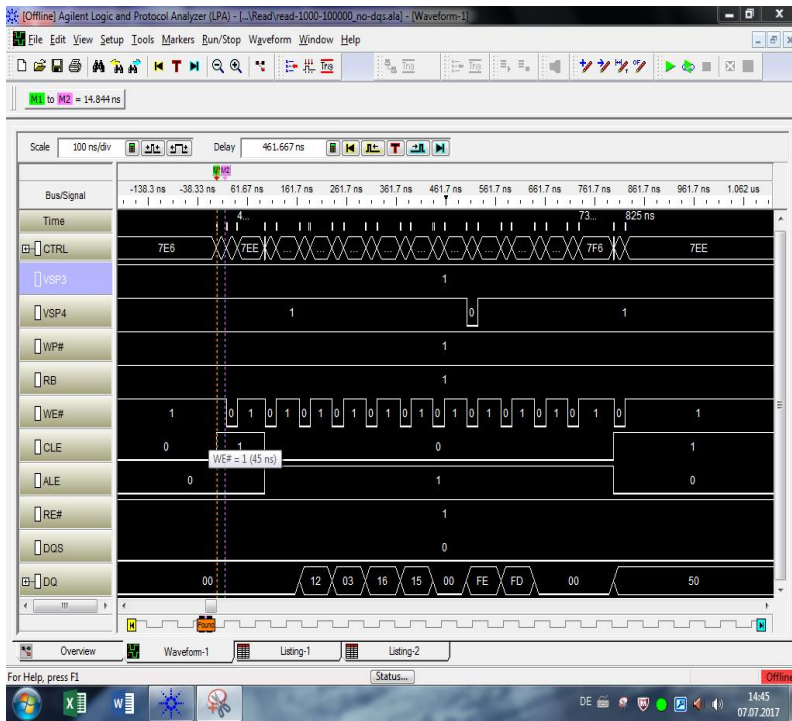


- BCH (Bose–Chaudhuri–Hocquenghem)
 - hard-decision decoding with read-retry
- LDPC – (Low-Density Parity Check)
 - supports soft-decision decoding with read-retry
- Adaptive LDPC
 - code changes throughout life of NAND
 - smaller (weaker) ECC when new
 - larger (stronger) ECC as NAND ages

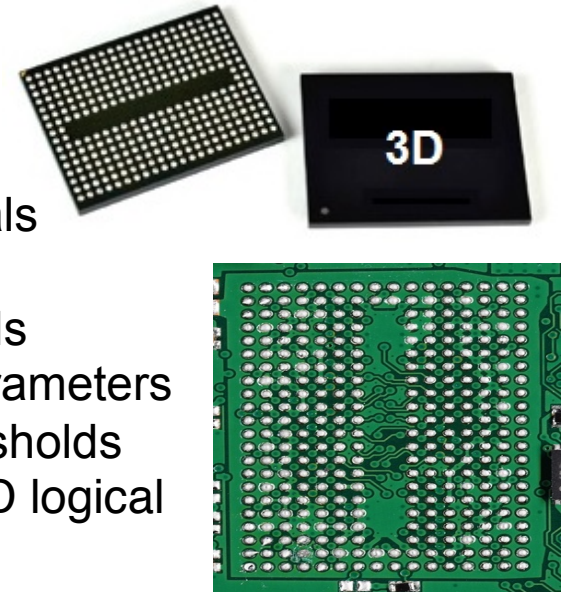


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Reading 3D NAND: New Challenges

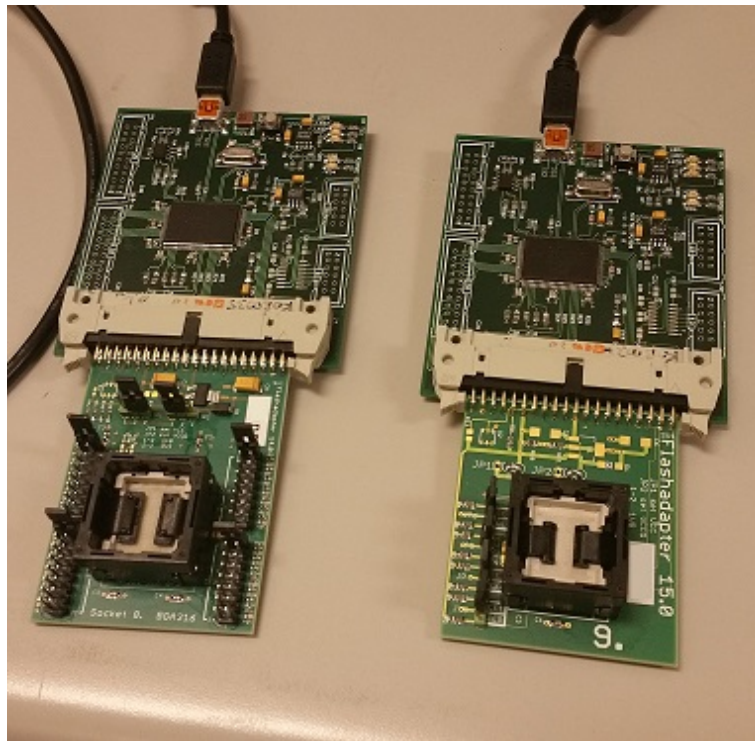


- Vendor Specific Signals
- Extended Addressing
- Proprietary Commands
- New Set Features parameters
- New Read-Retry thresholds
- Determining 3D NAND logical structure



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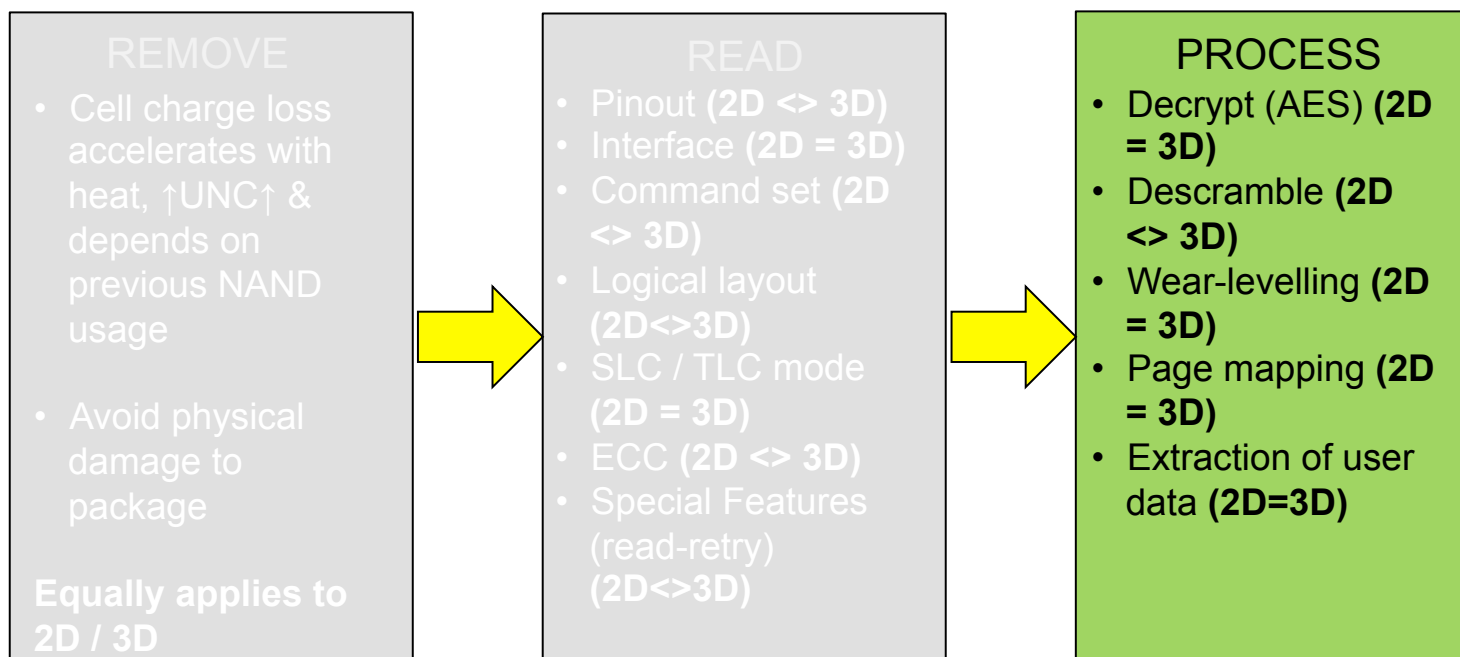
SSD Chip-Off: Read NAND



- Kroll Ontrack USB “FlashReader” custom hardware solution with interchangeable adapters
- Support for wide range of packages
- Dynamic core voltage control
- Split Vcc and VccQ
- Precise interface timing control



SSD Chip-Off: Process NAND



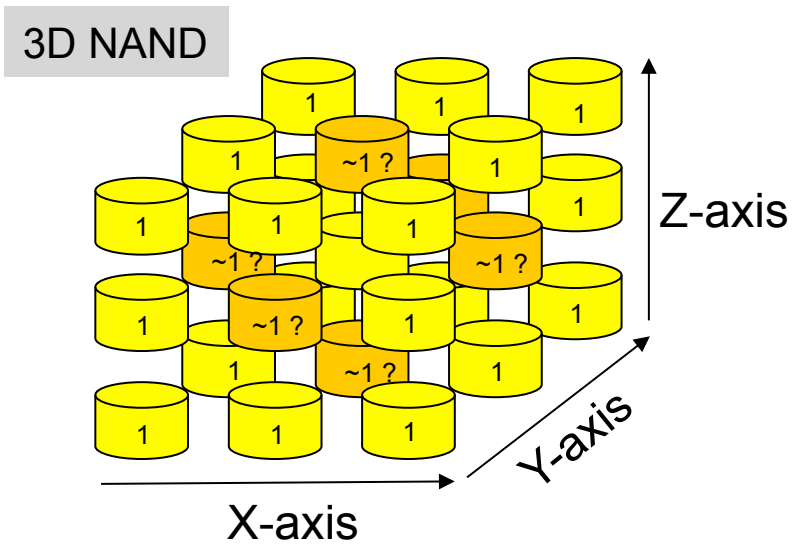
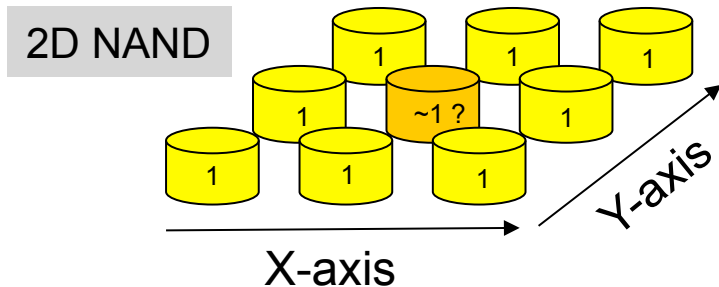


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Process 3D NAND: New Challenges

= cell programmed / erased with '1'

= victim cell, was programmed with '0'
...but reads closer to '1'



X, Y and Z-axis directional cell-to-cell interference requires new scrambling / de-correlation algorithm



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Summary

- A “Chip-Off” approach is vital for physical-level Erasure Verification on SSD plus some SSD failures mean “Chip-Off” the only way to recover data
- Noticeable rapid shift from 2D to 3D NAND in all solid-state applications - data recovery service providers need to keep on top of this technology
- 3D NAND introduces new challenges for both reading and processing raw data for chip-off data recovery and Erasure Verification
- Ongoing support from drive and controller manufacturers is crucial - reduces the research efforts needed to get customers’ data back and chip-off then becomes cost-effective



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Thank You!

Please visit us at booth #700

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