Challenges in Vertically Stackable Selectors for 3D Cross-Point Non Volatile Memories

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Outline

- Introduction and Background
  - 3D Cross Point Architecture – memory and selector
  - Selector Types

- NVM Device Development Challenges

- High-Throughput Experimentation Methodology
  - PVD Deposition and Etest
  - Test Vehicle Considerations

- Selector Case Studies
  - Tc screening vs composition
  - Electrical screening

- Summary
Selector devices are critical to eliminating sneak current paths
Disruptive selectors needed to address performance, density and reliability requirements
Survey of NVM Selector Device Options

<table>
<thead>
<tr>
<th></th>
<th>Selector Req’ts</th>
<th>MSM</th>
<th>Oxide-PN⁴</th>
<th>MIEC⁶</th>
<th>Metal-Oxide Schottky⁵</th>
<th>MIIM Bi-directional Varistor⁷</th>
<th>Chal OTS⁸</th>
</tr>
</thead>
<tbody>
<tr>
<td>Max Forward Current Density/Feature Size</td>
<td>~10⁶⁻⁷ A/cm²</td>
<td>~10⁻⁷ A/cm²</td>
<td>~5x10⁴ A/cm²@2V 0.5x 0.5um</td>
<td>~10⁵⁻⁸ A/cm²@1V ~80nm bot</td>
<td>3x10⁵ A/cm²@2V 2x2um</td>
<td>~3x10⁷ A/cm²@2.5V 250nm hole</td>
<td>Feasibility shown for 90nm PCM</td>
</tr>
<tr>
<td>J₁FB/J₁RB Ratio &amp; J₁V₁/J₄V₂ Ratio</td>
<td>&gt; 10⁵ &amp; &gt; 10³</td>
<td>~ 10³</td>
<td>~10⁴ ~100</td>
<td>~10⁴</td>
<td>2.4x10⁶ ~10³</td>
<td>~10⁴</td>
<td>Met PCM Req</td>
</tr>
<tr>
<td>Directionality</td>
<td>Uni or Bipolar</td>
<td>Bipolar</td>
<td>Unipolar</td>
<td>Bipolar</td>
<td>Unipolar</td>
<td>Bipolar</td>
<td>Bipolar</td>
</tr>
<tr>
<td>Switching Time/Endurance</td>
<td>&lt; 10ns/ &gt; 10⁸</td>
<td>&lt;10ns/10⁻⁷ns/ ?</td>
<td>10⁻¹⁰0ns/ ?</td>
<td>~ 1ns/ &gt; 10⁶</td>
<td>&lt; 1ns/ &gt; 10¹⁰</td>
<td>?</td>
<td>Feasibility shown for 90nm PCM</td>
</tr>
<tr>
<td>Deposition Temp/Thermal Stability</td>
<td>&lt; 400°C/ &gt; 400°C</td>
<td>&lt; 400°C/ &gt; 400°C</td>
<td>&lt; 400°C/ ?</td>
<td>200°C/ &gt; 400°C</td>
<td>250°C/ ?</td>
<td>300°C/ ?</td>
<td>&lt; 400°C/ Issue</td>
</tr>
<tr>
<td>Typical Materials/Stacks Used</td>
<td>Fab Friendly</td>
<td>Semiconductors</td>
<td>CuO/IZO NiO/IZO</td>
<td>Cu in Solid Electrolyte</td>
<td>Pt/TiO₂/ TiO₂ₓ/Pt</td>
<td>Pt/Ta₂O₃/TiO₂ /Ta₂O₃/Pt</td>
<td>As, Ge, Si, S, Se, Te, N</td>
</tr>
<tr>
<td>I-V Curves</td>
<td><img src="image1" alt="Graph" /></td>
<td><img src="image2" alt="Graph" /></td>
<td><img src="image3" alt="Graph" /></td>
<td><img src="image4" alt="Graph" /></td>
<td><img src="image5" alt="Graph" /></td>
<td><img src="image6" alt="Graph" /></td>
<td><img src="image7" alt="Graph" /></td>
</tr>
</tbody>
</table>

- Choice of selector devices in 3D Cross-point implementation is a trade-off between performance, reliability and ease of integration.
NVM Device Development Considerations

- Filamentary based
  - O-vacancies (ReRAM)
  - Me-ions (CBRAM)
- Non-filamentary based
  - Memristor-like
  - Vacancy modulated conductive oxides
  - MIEC Selectors
- Alternative NVMs

Material/Stack

Device Structure

- Current control and selection
  - 1T1R, 1R1R, 1D1R, 1R1R, 1R
- Cell design for enhanced performances

Electrical Operation

- Control of each step starting with forming
- Characterize performance vs yield vs data retention trade-offs as a function of electrical operation

Disruptive NVM memories/selectors need fast and comprehensive device screening/experimentation
PVD Site-Isolated Deposition and Test

Each site is an independent experiment

- Each layer can be deposited by 1 to 5 sputter sources
- Multiple layers can be deposited at one site
- Aperture defines area where material is deposited → areas are site isolated
- Shutters for Aperture and Target prevents cross-contamination between layers & targets
- Each site composition is physically and electrically characterized

- Rapid deposition and screening of compositionally diverse space of interest
### Test Vehicle Description

<table>
<thead>
<tr>
<th>Test Vehicle</th>
<th>Description</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>Unit Films on Blanket Wafer &lt;1 week</td>
<td>Materials screening, ALD and PVD unit process optimization and integration</td>
<td>- Saturation and growth curves, dep rate</td>
</tr>
<tr>
<td>Shadow Mask &lt;3 days</td>
<td>Measure I-V at RT before/after anneal</td>
<td>- Physical/electrical characterization</td>
</tr>
<tr>
<td>Primary Test Vehicle</td>
<td>Mushroom Like, BEL CD≥150nm, 1R1R, Single Bit/Mini-Array</td>
<td>- Pulse P/E Power</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- Read State Disturbance</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- P/E Power vs Time</td>
</tr>
<tr>
<td>Secondary Test Vehicle</td>
<td>Column/Pillar Like, TEL= BEL CD≥150nm, 1R1R and 1T1R, Single Bit/Mini-Array</td>
<td>- Data Retention</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- Endurance</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- Performance Variability</td>
</tr>
<tr>
<td>Tertiary Test Vehicle</td>
<td>Column/Pillar Like, TEL= BEL CD≥ Minimum 1R1R and 1T1R, Single Bit → Large Arrays</td>
<td>- Area Scaling</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- Integration and Yield</td>
</tr>
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<td></td>
<td></td>
<td>- MLC and ECC</td>
</tr>
</tbody>
</table>

*Ref: TY Liu 2013 ISSCC
NVM Selector Screening Methodology

- Material composition space for Chalcogenide glasses exhibiting threshold vs. memory switching can be rapidly screened for physical and electrical performance.
- Explore composition space of Group IV (Si, Ge), V (As) and VI (Se, Te) compounds to develop guideline of thermal stability, resistivity, optical bandgap and I-V characteristics

- Phase I – Composition vs. Thermal stability, crystallinity, resistivity, and optical bandgap
- Phase II – Composition vs. IV (Selected portion of Phase Diagram)

Selector development is based on High-Throughput-Experimentation deposition and characterization methodology
Phase I: Rapid Screening of $R_s$ vs Temperature

Varying composition $AxByCz$

Rapid evaluation of the composition space for Tc enables the use of Tc as a pre-filter for promising selector candidates.
Phase II: Electrical Characterization

- DCIV
  - Level 1 screening
  - All splits

- Pulsed IV
  - Level 2 screening
  - Selected splits

- Endurance
  - Level 3 screening
  - Champion splits

Increasingly advanced electrical characterization used to realize screening promising selector candidates
Summary

• The move towards 3D Cross-point architecture for non-volatile memories has resulted in a need for disruptive memory and selector devices
  • Choice of selector devices is a trade-off between performance, reliability and ease of integration (fab-friendliness)

• Realization of disruptive NVM memories/selectors needs fast and comprehensive device screening/experimentation

• We propose a High-Throughput-Experimentation methodology that enables rapid new materials development and characterization for:
  • Compositionally wide material space
  • Increasingly complex electrical performance characterization

• IMI has successfully collaborated with customers to realize novel devices using this methodology

  • Acknowledgments: C Chen, J Watanabe and Customer+IMI collaboration teams