Comparison of NAND Flash Functionality with Internal Probing and Waveform Analysis

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Overview

- NAND flash SSD overview and logical vs. physical addressing
- Important test and analysis points
- NAND flash internal waveform analysis
  - Jet-etching and probing
  - Internal waveforms and states
- SSD controller to NAND flash interface
  - Interposing for testing
  - Standards (ONFI, Toggle) and customizations
- VNAND
Overview

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NAND Flash SSD Overview

- A port for host requests, such as SATA, USB, PCIe, eMMC, UFS, etc.
- Controller and many NAND flash memory devices
- Controller translates host requests to NAND flash memory requests
- The host cannot control the physical addressing (i.e., NAND flash).

Logical Address:
0
1
...
4000000
...

Physical Address:
Channel 1, 2, ...
Chip 1, 2, ...
Block 1, 2, ...
Page 1, 2, ...
Column 1, 512, ...
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Important Test and Analysis Points

- Host side testing and analysis can be done
  - Simple host benchmarking and testing SW
  - Protocol analyzer (e.g., SATA analyzer)
  - Limited (access rates, speculation, etc.)

SATA Protocol Analysis

SATA I/F Benchmarking

Toshiba SSD
Important Test and Analysis Points

- Physical side has some interesting points for test and analysis
  - Internal flash operations (e.g., WL, BL, SL, etc.)
  - Controller to flash interface (ONFI, Toggle)
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NAND Flash Waveform Analysis

- Jet etch to expose die for FIB pad placement for IC probing
- Challenges can include:
  - packaging obstructions
  - BGA to programmer translation
  - device repackaging (e.g., SD card) for direct NAND flash connectivity to programmer.

Cut lead frame
Bottom side
BGA
Re-wiring NAND flash in SD card
FIB pad placement challenges with shrinking NAND flash:

- Requires initial circuit extraction from the NAND flash IC
- Metallization thickness, M1 vs M2 for FIB connection
- BL pitch to get BL signals!
NAND Flash Waveform Analysis

- Fine tuning of programming during ISPP
- Raised BL voltage during programming pulses before inhibit
- Increased BL voltage during verify and small voltage difference (sensing scheme)
NAND Flash Waveform Analysis

- TLC verify extends programming time (~2x pulse-to-pulse)
- Sensing during verification produces small BL differences

SanDisk/Toshiba
15 nm
TLC

Middle page program

Small BL difference

160 us
NAND Flash Waveform Analysis

- Reading is simpler in MLC vs. TLC
- TLC requires many more read voltages
NAND Flash Waveform Analysis

- Variations in erase algorithms
- Single large pulse and programming

Micron 34 nm MLC

Pre-erase programming

Soft programming

Samsung 42 nm MLC

SanDisk/Toshiba 43 nm MLC

Soft programming
NAND Flash Waveform Analysis

- Variations in erase algorithms
- Multiple pulses and verification

SanDisk/Toshiba 19 nm MLC

SanDisk/Toshiba 15 nm TLC
NAND Flash Waveform Analysis

- 2-bit change between states implemented across the industry around the 5x/4x nm node
- Changed to single bit change from state to state
NAND Flash Waveform Analysis

- 2-bit change between states implemented across the industry around the 5x/4x nm node
- Changed to single bit change from state to state – including TLC

SanDisk/Toshiba 15 nm TLC
Simpler programming for 2 bits/cell

LSB page and MSB page can be programmed at different times (page addressing)
TLC devices can require all 3 pages of data together (WL addressing), multiple times.

Programming Steps and Memory Threshold Voltage Distribution and Placement
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Controller to NAND Flash Analysis

- Simple clip-on interposers for TSOP-48 NAND flash
- BGA packages are more complex
- Case-by-case: many different standard pin-outs
- Can also be non-standard pin-out; would need to first reverse engineer pin-outs

*SATA connection to Protocol Analyzer and PC*

*Testing and analysis of HGST SATA SSD*
Controller to NAND Flash Analysis

- ONFI and JEDEC Toggle NAND Standards
- Customizations:
  - Raw NAND controllers
  - BGA layouts
  - Command sets
- Example of custom commands, SSD Boot-up:
  
<table>
<thead>
<tr>
<th>Opcode</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x70</td>
</tr>
<tr>
<td>0xEF</td>
</tr>
<tr>
<td>0xC3</td>
</tr>
<tr>
<td>0x28</td>
</tr>
<tr>
<td>0xE7</td>
</tr>
<tr>
<td>0x55</td>
</tr>
</tbody>
</table>

Source: Open NAND Flash Interface Specification, Rev 4.0

*Testing and analysis of HGST SATA SSD
Controller to NAND Flash Analysis

- Addressing dependent on NAND flash device
- Example typical 5 cycle addressing with column, page, block/plane (SanDisk SSD):

<table>
<thead>
<tr>
<th></th>
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<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>CA7</td>
<td>CA6</td>
<td>CA5</td>
<td>CA4</td>
<td>CA3</td>
<td>CA2</td>
<td>CA1</td>
<td>CA0</td>
</tr>
<tr>
<td>2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>PA7</td>
<td>PA6</td>
<td>PA5</td>
<td>PA4</td>
<td>PA3</td>
<td>PA2</td>
<td>PA1</td>
<td>PA0</td>
</tr>
<tr>
<td>4</td>
<td>BA6</td>
<td>BA5</td>
<td>BA4</td>
<td>BA3</td>
<td>BA2</td>
<td>BA1</td>
<td>BA0</td>
<td>PL</td>
</tr>
<tr>
<td>5</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Page address
TLC and 3D NAND flash devices can greatly disrupt this
- Page vs. WL + L/M/U bit command prefix
- More address cycles will be needed
- Locations of changes relative to standard addressing signals:
Controller to NAND Flash Analysis

- Logical blocking with multi-plane operations is the usual industry approach
- Reduced signalling with Status Check commands instead of Ready/Busy lines
- Example controller to NAND flash transactions excerpt (SanDisk SSD):

<table>
<thead>
<tr>
<th>Sample #</th>
<th>Start</th>
<th>End</th>
<th>Cmd</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>Command</th>
<th>Plane</th>
<th>Block</th>
<th>Page</th>
<th>Column</th>
<th>Data</th>
</tr>
</thead>
<tbody>
<tr>
<td>28</td>
<td>04:56:00</td>
<td>04:56:06</td>
<td>70</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>00</td>
<td>Status check + 4</td>
<td>0</td>
<td>68</td>
<td>96</td>
<td>0</td>
<td>1D AD 92 57 A8 64</td>
</tr>
<tr>
<td>17724</td>
<td>04:58:41</td>
<td>04:58:42</td>
<td>11</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Data end</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>17729</td>
<td>04:58:41</td>
<td>04:58:43</td>
<td>70</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>00</td>
<td>Status check</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>17736</td>
<td>04:58:44</td>
<td>04:58:46</td>
<td>70</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>00</td>
<td>Status check</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>17744</td>
<td>04:59:05</td>
<td>04:59:06</td>
<td>81</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>00</td>
<td>Program multi-plane</td>
<td>1</td>
<td>66</td>
<td>96</td>
<td>0</td>
<td>60 8D 83 48 DC 4E</td>
</tr>
<tr>
<td>35433</td>
<td>04:59:07</td>
<td>04:59:08</td>
<td>10</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Data end</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>36733</td>
<td>04:59:08</td>
<td>04:59:10</td>
<td>70</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>00</td>
<td>Status check + 4963</td>
<td>0</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>77526</td>
<td>05:00:18</td>
<td>05:00:20</td>
<td>70</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>00</td>
<td>Status check + 270</td>
<td>0</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- Industry preferences for certain commands, addressing, wear leveling, garbage collection, disturb management, etc. will be disrupted with TLC and 3D NAND
- New industry best practices going forward TBD
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VNAND

- 3D array and periphery configurations
  - Side-by-side
  - Stacked array over circuitry
  - Other future considerations (TSV)

- NAND flash standards
  - Pin-outs
  - Addressing
  - Control
Thank you

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