Media Management for High Density NAND Flash Memories

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Outline

- NAND Flash Scaling Trends
- LDPC with Hard and Soft Decision Decoding
- Adaptive Code Rates
- Read Voltage Calibration
- Redundant Silicon Elements
- Summary
NAND Scaling Trends

- 3D NAND may extend beyond 100 layers
- 3D NAND extends scaling towards 1Tb die capacity

- Required ECC for SSD-grade endurance exceeds 60b/1KB for 2D TLC
- 3D NAND relies on strong ECC to make TLC mainstream for SSDs
## NAND Impairments

<table>
<thead>
<tr>
<th>Impairment</th>
<th>Effect</th>
<th>Mitigation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Program/Erase Cycling</td>
<td>Voltage shift/widening</td>
<td>ECC</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Read Voltage Calibration</td>
</tr>
<tr>
<td>Retention</td>
<td>Voltage shift/widening</td>
<td>ECC</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Read Voltage Calibration</td>
</tr>
<tr>
<td>Media Defects</td>
<td>Page, block, plane, die failure</td>
<td>Redundant Silicon Elements</td>
</tr>
</tbody>
</table>

- Presented Flash media management algorithms can help to mitigate Read Disturb and Intercell Interference as well
Low-Density Parity Check (LDPC) Codes

- Defined by a sparse (low density) parity check matrix $H$
- Are represented with a bi-partite graph
- Support hard and soft decision decoding

$$H = \begin{bmatrix}
1 & 1 & 0 & 1 & 0 & 1 \\
0 & 1 & 1 & 1 & 1 & 0 \\
1 & 0 & 1 & 0 & 1 & 1 \\
\end{bmatrix}$$

Bi-Partite Graph:

- Bit nodes: $b_1, b_2, b_3, b_4, b_5, b_6$
- Check nodes: $c_1, c_2, c_3$
NAND Flash Memory compares read voltage with read reference voltage to generate hard decision.

- One reference voltage for LSB page, 2 reference voltages for MSB page.
- Hard decision is used for decoding.
- Sequence of read operations with different read reference voltages to generate soft decision
- Computation of soft information (LLRs) based on multiple read decisions
- LDPC decoder uses soft decision during error recovery
Hard/Soft LDPC vs. BCH

- Soft-decision LDPC decoding has significantly better error correction than BCH decoding
Experimental Benefit of Soft LDPC

- Measured with controller silicon and firmware for 15/16nm MLC flash
- Significant error rate improvement with soft LDPC decoding
Adaptive Code Rates

- **Beginning of Life**: use less ECC to increase overprovisioning
- **End of Life**: increase ECC to maintain reliability

**Conventional Error Correction**: Stores fixed ECC in spare field

**Adaptive ECC (BOL)**: Stores ECC in a portion of spare field and increase OP

**Adaptive ECC (EOL)**: Stores ECC in spare field and uses some of the NAND page

Adaptive ECC allows for more free space @ BOL = More OP and less write amplification
Switching Code Rates

- Measured with controller silicon and firmware for 15/16nm MLC flash
- Multiple LDPC codes cover wide RBER range
- As NAND flash ages, controller switches to the next stronger code
- Read performance improves, since stronger LDPC codes decode data faster
Read Voltage Calibration

- Optimum read voltages shift as a function of endurance, retention and read disturb
- Optimized read voltages reduce retry rate and extend endurance
Experimental Results: Read Voltage Calibration

- Measured with controller silicon and firmware for 3D flash
- Significant improvement in RBER after read voltage calibration
Media Failures

- Pages, blocks, planes or the whole die can fail
- ECC cannot recover data from such catastrophic failures
- Need RAID-like protection inside SSD
RAISE™: Redundant Array of Independent Silicon Elements

- RAID-like data protection within the drive
- Write data across multiple dies with additional protection
- Corrects full page, block or die failures when all soft LDPC steps fail
SSD Controller: Block Diagram

SSD Controller

Data Management

Host

Host Interface

FTL

ECC

LDPC Encoder

LLR Generation

LDPC Decoder

Firmware: Data and Media Management

Write path

Read path

Read/Write

Flash Interface

NAND Flash devices

Controller
Multi-Level Error Correction

- Hard-decision LDPC decoding is on-the-fly error correction method
- Progressively apply stronger decoding methods such as soft-decision LDPC decoding and signal processing
- Specialized noise handling techniques for P/E cycling, retention, read disturb, etc.
- Optimize time-to-data
Conclusion

- Latest memory geometries demand intelligent NAND management features
- 3D NAND will still rely on strong ECC and advanced NAND management features to make TLC mainstream for SSD applications
Thank You! Questions?

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