Advanced Controller Technology for 3D NAND Flash

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Outline

- The Reliability Issues of 3D NAND Flash
- The Architecture of Error Handling Technology
- Error Correction Technology
- Comparison between ECC engines
- Reliability of SSD with 3D NAND Flash memory
- Conclusion
Outline

• The Reliability Issues of 3D NAND Flash
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The Reliability Issues of 3D NAND

- Fast de-trapping of programmed electron
- Layer Dependency
- Different erase mechanism from 2D NAND
- Different retention behavior from 2D NAND
- Weak read disturb immunity
- Weak program disturb immunity
Outline

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Error Handling Tech. in Controller

- **Digital Signal Processors:**
  - Reduce Error.
  - Collect/transfer the channel info.

**NAND Flash**

**NAND I/O Interface**

**Digital Signal Processor**
- HRE Eliminator
  - Vth Distribution Construction
  - Random Noise Cancellation
  - HRE Statistic Collection
  - Read Level Optimization
- Reliability Information Processor
  - Data Reconstruction
  - Digital Signal Translation
  - Statistical Analyzer
- Noise Cancellation
- Reliability Information Scaling
- Adaptive LLR Calculation
- Error Characterization
- Error Probability Analyzer
- Information Scaling

**Firmware**
- Health Monitoring
- Flash Parameter optimization
- Advanced Protection

**BCH/SECC/LDPC/Matrix ECC**
Error Handling Tech. in Controller

**Firmware:**
- Judge the info. from DSP/ECC.
- Adaptively control ECC engine.
- Adaptively control NAND Flash.
- Adaptively change the data Structure.
Error Handling Tech. in Controller

- ECC Engine:
  - Low Power.
  - Low Cost.
  - Excellent Correction Strength.
Error Handling Tech. in Controller

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• The Reliability Issues of 3D NAND Flash
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• Conclusion
Which Way to Go?
Which Way to Go?
Which Way to Go?
Which Way to Go?
Which Way to Go?

Power consumption
Which Way to Go?

Power consumption

Cost
Which Way to Go?

Power consumption

Cost

HRE

LDPC

BCH
Which Way to Go?

Power consumption

Cost

HRE

LDPC

BCH
Which Way to Go?

- Power consumption
- Cost
- HRE
- LDPC
- BCH
- Correction strength of BCH

# of Error bits vs. Probability
Phison Provides a NEW WAY for ECC
Novel Design of LDPC Technology
Novel Design of LDPC Technology
Outline

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## Comparison between ECC tech

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<th>Conventional LDPC</th>
<th>BCH</th>
</tr>
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<tbody>
<tr>
<td>Decoding Algorithm</td>
<td>Probability Based</td>
<td>Algebraic Based</td>
</tr>
<tr>
<td>Guaranteed Correction Strength</td>
<td>No</td>
<td>Yes</td>
</tr>
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<td>Easy</td>
<td>Hard</td>
</tr>
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<td>Performance of Hard Decoding</td>
<td>Similar to BCH</td>
<td>Code Length * (1-code rate) / Degree of polynomial</td>
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## Comparison between ECC of Phison

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</table>
## ECC Technology of Phison

<table>
<thead>
<tr>
<th>ECC Type</th>
<th>Correction Strength</th>
<th>Gate Count</th>
<th>Technology node (nm)</th>
<th>Support NAND</th>
<th>Q3' 2016</th>
<th>Q4' 2016</th>
<th>2017</th>
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</thead>
<tbody>
<tr>
<td>1K BCH</td>
<td>72/1K</td>
<td>260K</td>
<td>55/40/28</td>
<td>2D/3D MLC/TLC</td>
<td>Applied for USB/SD/eMMC/SSD</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2K BCH</td>
<td>120/2K</td>
<td>540K</td>
<td>55</td>
<td>2D/3D MLC/TLC</td>
<td>Applied for SSD</td>
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<td></td>
</tr>
<tr>
<td>SECC</td>
<td>95&amp;135/1K</td>
<td>300K</td>
<td>40</td>
<td>2D/3D MLC/TLC/QLC</td>
<td>Applied for SD/eMMC/UFS/SSD</td>
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</tr>
<tr>
<td>4K LDPC Lite</td>
<td>72&amp;150/1K</td>
<td>0.7M</td>
<td>40</td>
<td>2D/3D MLC/TLC/QLC</td>
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<td>4K LDPC</td>
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<td>28</td>
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<td></td>
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<tr>
<td>Matrix ECC</td>
<td>-</td>
<td>300K</td>
<td>55/40/28</td>
<td>2D/3D MLC/TLC/QLC</td>
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<td>PS3111-S11 SATA Controller</td>
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<tr>
<td>• Economy SATA3 SSD with Good performance and decent cost</td>
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<tr>
<td>• Design for OEM/embedded applications</td>
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<td>• Support DEVSLP &amp; LDPC</td>
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SATA 2.5" M.2 2280 M.2 2242
Hardware Architecture of LDPC Lite

NAND Flash

NAND Interface

DSP
- Data Reconstruction
- Digital Signal Translation
- Statistical Analyzer

Noise Cancelation
- Reliability Information Scaling
- Adaptive Channel Information Calculation

Firmware

LLR table

DIS Processor
- Error Characterization
- Error Probability Analyze
- Information Scaling

Novel DECODER
- Input Memory
  - HB
  - SB
- Low Power Engine
- Early Termination
- Check Node Unit
- Variable Node Unit
- Temporary Memory

Flash Memory Summit 2016
Santa Clara, CA
Ultra Low Power Consumption

![Graph showing power consumption vs. number of error bits](image)

- BCH
- LDPC Lite
- SECC

Flash Memory Summit 2016
Santa Clara, CA
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<td>Yes</td>
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<tr>
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Ultra Low Power Consumption

![Graph showing power consumption versus number of error bits. The graph compares BCH, LDPC Lite, and SECC.](image-url)
Hardware Architecture of SECC

NAND Flash

NAND Interface

DSP
- Data Reconstruction
- Digital Signal Translation
- Statistical Analyzer
- Noise Cancellation
- Reliability Information Scaling
- Adaptive Channel Information Calculation

Firmware

Novel DECODER
- Memory Interface
  - HB
  - SB
- Temporary Memory
- Error Correct Engine
- Channel Error Estimator
- Flow Control Unit
- Error Trapping Detector
- Early Termination

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34
Correction Capability of SECC

- ~70%
- ~30% increase
- ~70% increase

Graph showing UBER vs. RBER with different error correction methods:
- BCH 72bits/1K
- Novel ECC
- Soft Decoding

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Ultra Low Power Consumption

![Graph showing power consumption vs. number of error bits]

- BCH
- LDPC Lite
- SECC

Power (mW)

Number of Error Bits / 1K (#)
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Reliability Improvement of 3D NAND

![Graph showing the max number of error bits per 1K vs. PE cycles for different time periods: 0 month, 3 months, 6 months, 9 months, and 12 months. The graph highlights the impact of BCH/HB of LDPC Lite.]
Reliability Improvement of 3D NAND

BCH/HB of LDPC Lite

HB of SECC + DSP

2X Extended
Reliability Improvement of 3D NAND

>3X Extended

SB of SECC + DSP (PS5008) / LDPC Lite +DSP (PS3111)

HB of SECC + DSP

BCH/HB of LDPC Lite

Max number of Error bit per 1K

0 month
3 months
6 months
9 months
12 months

RF cycles
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Conclusion

• The power consumption of the LDPC lite and SECC engine are only 1/3 than the convention BCH.
• With the novel design of decoding algorithm, the cost of LDPC can be reduced effectively.
• The endurance of 3D NAND Flash can be 3X more extended by SECC and LDPC lite with DSP engine.
Meet us at booth 714 & 716

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