Management Schemes of Hybrid SSDs with SLC/MLC Flash Memory: A Survey

Ahmed Izzat Alsalibi*, Putra Sumari and Mohammed Azmi Al-Betar

Ahmed Izzat Alsalibi and Putra Sumari are with School of Computer Science, Universiti Sains Malaysia, Pulau penang 11800, Malaysia. Corresponding author email: ahmed.salibi@gmail.com.
Mohammed Azmi Al-Betar with Department of Information Technology, Al-Huson University College, Al-Balqa Applied University, 50, Al-Huson, Irbid, Jordan.
Introduction and Background
• Advantages of SSD over HDD
• SSD Architecture
• Flash Translation Layer (FTL)
  - Address Translation - Garbage Collection (GC) - Wear Leveling (WL)
• Comparison Between SLC, MLC and TLC

Hybrid SSD Schemes
• Schemes using SLC as a buffer (SLC-Buf)
• Schemes Using Both SLC and MLC as a Buffer (SLC/MLC-Buf)
• Schemes Using External Memory as a Buffer (ExtM-Buf)
• Schemes without a Buffer (No-Buf)

Conclusion and Possible Future Directions
Advantages of SSD over HDD

- Low power consumption
- Higher flexibility to external shock
- High random access performance
A typical SSD Architecture
A typical SSD Architecture
Flash Translation Layer (FTL)

- FTL typically provide three software components:
  - Address Translation
  - Garbage Collection (GC)
  - Wear Leveling (WL)
Garbage Collection

(a) Flash memory before implementing GC at block 1
(b) Flash memory after implementing GC at block 1

- Invalid Page
- Valid Page
- Free page
Wear Leveling

(a) Flash memory without wear leveling technique.

(b) Flash memory with wear leveling technique.

- Green: Block with erase cycles
- Red: Wear-out Block
- White: Block without erase cycles
Comparison Between SLC, MLC and TLC

(a) SLC

(b) MLC

(c) TLC
Comparison Between SLC, MLC and TLC

(Dong and Xie 2011) (Hsieh et al. 2015)

<table>
<thead>
<tr>
<th>Features</th>
<th>SLC</th>
<th>MLC</th>
<th>TLC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Density</td>
<td>Low</td>
<td>High</td>
<td>Very high</td>
</tr>
<tr>
<td>Cost per bit</td>
<td>High</td>
<td>Low</td>
<td>Very low</td>
</tr>
<tr>
<td>Page size</td>
<td>2K bytes</td>
<td>4K bytes</td>
<td>16K bytes</td>
</tr>
<tr>
<td>Block size</td>
<td>128K bytes</td>
<td>512K bytes</td>
<td>1.5M bytes</td>
</tr>
<tr>
<td>Page read</td>
<td>20 μs</td>
<td>50 μs</td>
<td>100 μs</td>
</tr>
<tr>
<td>Page write</td>
<td>350 μs</td>
<td>900 μs</td>
<td>2400 μs</td>
</tr>
<tr>
<td>Block erase</td>
<td>1500 μs</td>
<td>2000 μs</td>
<td>3000 μs</td>
</tr>
<tr>
<td>W/E Cycles</td>
<td>100,000</td>
<td>10,000</td>
<td>&lt; 1,000</td>
</tr>
<tr>
<td>Electrical Voltage</td>
<td>3.3V</td>
<td>3.3V</td>
<td>3.3V</td>
</tr>
<tr>
<td>Electrical Current</td>
<td>15 mA</td>
<td>15 mA</td>
<td>15 mA</td>
</tr>
<tr>
<td>Price (USD/GB)</td>
<td>4.92</td>
<td>1.7</td>
<td>0.63</td>
</tr>
</tbody>
</table>
Organizations of Hybrid SSD Schemes

Hybrid Flash Memory Schemes

Buffer Location

Volatile Memory
- RAM

Non-Volatile Memory
- SLC
- MLC
- SLC and MLC

Mapping Techniques

Page-Level
- Hybrid

Block Level

Partitioning Techniques

Hard
- Soft
Hard vs. soft partitioning

(a) Hard Partitioning

(b) Soft Partitioning
# Schemes using SLC as a buffer (SLC-Buf)

<table>
<thead>
<tr>
<th>Schemes</th>
<th>Basic Idea</th>
<th>Buffer Location</th>
<th>Mapping Technique</th>
<th>Partitioning</th>
</tr>
</thead>
<tbody>
<tr>
<td>Chang (Chang, 2008)</td>
<td>Passing the hot data to SLC and cold data in MLC. The small write request should be manipulated by SLC.</td>
<td>SLC</td>
<td>Page-Level</td>
<td>Block-Level</td>
</tr>
<tr>
<td>Hierarchical FAST-MS (Jung and Song, 2009)</td>
<td>Passing the write data to a non-volatile buffer, which located at SLC portion, to avoid performing write and erase operation at MLC.</td>
<td>SLC</td>
<td>Log-Based Hybrid</td>
<td>Log-Based Hybrid</td>
</tr>
<tr>
<td>Bypassing (Im and Shin, 2009)</td>
<td>Using the SLC as a log buffer and the MLC as a data block.</td>
<td>SLC</td>
<td>Page Level</td>
<td>Block Level</td>
</tr>
<tr>
<td>Combo FTL (Im and Shin, 2010)</td>
<td>Using small size of SLC for hot data and large size of MLC for cold data.</td>
<td>SLC</td>
<td>Page Level</td>
<td>Block-level</td>
</tr>
<tr>
<td>Hybrid Scheme (Nam et al., 2010)</td>
<td>Using small size of SLC for hot data and large size of MLC for cold data.</td>
<td>SLC</td>
<td>Page-level</td>
<td>Block-level</td>
</tr>
</tbody>
</table>
Architecture of hybrid storage combined SLC/MLC flash memory for Chang’s scheme

Chang 2010
Advantages and Disadvantages of (SLC-Buf)

• **Advantages**
  Increasing the performance of SSD in terms of speed.

• **Disadvantages**
  Using small size of SLC as a buffer to serve the hot data, thus the SLC portion will wear out quickly and that will affect the overall reliability of SSD.
<table>
<thead>
<tr>
<th>Schemes</th>
<th>Basic Idea</th>
<th>Buffer Location</th>
<th>Mapping Technique</th>
<th>Partitioning</th>
</tr>
</thead>
<tbody>
<tr>
<td>Soft Partitioning (Jimenez et al. 2012)</td>
<td>Using soft partitioning technique to move the physical location of the buffer either to SLC or to MLC based on their wears.</td>
<td>SLC and MLC</td>
<td>Hybrid FTLs</td>
<td>Hybrid FTLs</td>
</tr>
<tr>
<td>Phoenix (Jimenez et al. 2013)</td>
<td>Reusing the MLC blocks that have been worn out as SLC blocks. Using the fact that MLC blocks become unreliable can still reliably be used to store a single bit per cell.</td>
<td>SLC and MLC</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>FlexFS (Lee and Kim 2014)</td>
<td>Taking a benefit from flexible programming provided by MLC to provide ability for each cell to be programmed as SLC or MLC mode.</td>
<td>SLC and MLC</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>RR-FDCA (Hachiya et al. 2014)</td>
<td>Taking a benefit of TLC and adding it to hierarchy of hybrid SSD in order to decrease the cost.</td>
<td>MLC</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>
Architecture of hybrid storage combined SLC/MLC flash memory for soft partitioning scheme (Jimenez et al. 2012)
Advantages and Disadvantages of (SLC/MLC-Buf)

- Advantages
  - More reliable
  - More flexible
  - Cost efficient
- Disadvantages
  - More complex
<table>
<thead>
<tr>
<th>Schemes</th>
<th>Basic Idea</th>
<th>Buffer Location</th>
<th>Mapping Technique</th>
<th>Partitioning</th>
</tr>
</thead>
<tbody>
<tr>
<td>Yim’s scheme</td>
<td>Using volatile RAMs and non-volatile RAMs as a write buffer, and using different types of flash memories in order to reduce the overall storage cost.</td>
<td>VRAM and NVRAM</td>
<td>VRAM SLC</td>
<td>Hard</td>
</tr>
<tr>
<td>HFTL</td>
<td>Managing both SLC and MLC connected to each others using parallel pattern. The short and long write request will passed to MLC and SLC respectively.</td>
<td>DRAM Block Level</td>
<td>Page Level</td>
<td>Hard</td>
</tr>
<tr>
<td>PH-SSD</td>
<td>Dividing the SSD to three categories: PRAM used as a primary updating area, SLC used as a secondary updating area, and MLC used as a main storage area.</td>
<td>PRAM Page Level</td>
<td>Page Level</td>
<td>Hard</td>
</tr>
<tr>
<td>DABC-NV</td>
<td>Using two types of memory as buffer cache: non-volatile RAM and volatile RAM.</td>
<td>VRAM and NVRAM</td>
<td>VRAM MLC</td>
<td>Hard</td>
</tr>
</tbody>
</table>
Architecture of hybrid storage combined SLC/MLC flash memory for Yim’s scheme (Yim 2005)
Advantages and Disadvantages of (ExtM-Buf)

• Advantages
  - High speed
• Disadvantages
  - High price
  - Losing data in case of power outage
## Schemes without a Buffer (No-Buf)

<table>
<thead>
<tr>
<th>Schemes</th>
<th>Basic Idea</th>
<th>Buffer Location</th>
<th>Mapping Technique</th>
<th>Partitioning</th>
</tr>
</thead>
<tbody>
<tr>
<td>AFVM (Sung and Kim, 2012)</td>
<td>Exploiting the symmetry of SLC and MLC flash memory in their service time characteristics. The frequently writes operations with small size will be resided into SLC portion and the seldom writes operations with large size will be resided into MLC portion.</td>
<td>No Buffer</td>
<td>Device Mapper</td>
<td>Device Mapper</td>
</tr>
<tr>
<td>Hybrot (Murugan and Du, 2012)</td>
<td>Adapting the flow of hot data to the SLC and MLC regions in a systematic manner instead of using the SLC portion as a cache or log buffer for the MLC portion.</td>
<td>No Buffer</td>
<td>Page Level</td>
<td>Block Level</td>
</tr>
<tr>
<td>AHDM (Batni and Safaci, 2014)</td>
<td>Dividing the data to hot and warm data and identifying them using two LRU queues. It is based on dynamic WL (Yun et al., 2012).</td>
<td>No Buffer</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>HySSD (Oh, Lee, Choi, Lee and Noh, 2013a)</td>
<td>Passing the hot data to SLC and cold data to TLC.</td>
<td>No Buffer</td>
<td>Page Level</td>
<td>Page Level</td>
</tr>
</tbody>
</table>
Architecture of hybrid storage combined MLC/TLC flash memory for HySSD scheme by Oh et al., 2013.
Advantages and Disadvantages of (No-Buf)

- **Advantages**
  - Cost efficient
  - More flexible

- **Disadvantages**
  - Low performance
Conclusion and Possible Future Directions

• There are several open research trends that have already started on the ground. These future directions are summarized as follow:
  
  - Exploitation Trade-off Among SLC, MLC, and TLC.
  - Use Adaptive Parameters for the Future Software Schemes of Hybrid SSD Devices.
  - Use File-System-Level Information in Software Schemes of the Hybrid SSD.
  - Standardize the Simulators for Evaluation Purposes.
  - Build a Standard Benchmark for Comparison Purposes.
Thank you!