High Performance, FPGA-Optimized LDPC for Storage

Helen Tarn
Sr. Engineering Manager
Xilinx Inc.
BCH codes are running out of steam
  • Can't take advantage of soft-data
  • Performance is limited to the Shannon limit for a hard channel

LDPC codes
  • Near Shannon-limit performance
  • Take advantage of soft-data
  • Good implementations of LDPC codes are low power and cost effective

No standards for LDPC in storage space

Code “growth” technology with best-in-class coding performance at very low cost
DSP work is focused on the LDPC encoder, decoder and statistics processing below.
Xilinx LDPC Features

- Best-in-class code performance near Shannon limit
- Achieved low error floor under $10^{-15}$ with proprietary optimization method
- Support for code rate change on-the-fly
- Support both hard decision and soft decision decoding
- High throughput and low latency performance
- Scalable architecture supporting various options
- FPGA optimized for minimal area/power
- Provides decoder status and statistics interfaces
<table>
<thead>
<tr>
<th>Feature</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Codeword Length</td>
<td>1K Bytes + parity</td>
</tr>
<tr>
<td>Code Rate</td>
<td>Various options above .89</td>
</tr>
<tr>
<td>Rate switching on-the-fly</td>
<td>✓</td>
</tr>
<tr>
<td>Error Floor</td>
<td>Better than $10^{-15}$</td>
</tr>
<tr>
<td>Two Step Decoding</td>
<td>✓</td>
</tr>
<tr>
<td>Early Termination</td>
<td>✓</td>
</tr>
<tr>
<td>Device Supported</td>
<td>Ultrascale, 7-series</td>
</tr>
<tr>
<td>Clock Rate</td>
<td>400MHz</td>
</tr>
</tbody>
</table>
Advanced code construction methodology for best code performance
Achieved low error floor using proprietary optimization technique
Near Shannon limit performance
LDPC v.s. BCH Performance

- Codeword length = 1K User Bytes + 10.7% parity
- BCH: T=70
Error Floor Free Performance

![Graph showing the relationship between Coded Bit Error Rate and SNR (dB). The graph plots a curve that decreases as SNR increases, indicating improved performance.]
Error Correction Capability

- >3x Average Bit Errors Corrected using LDPC Soft Decision Decoding

<table>
<thead>
<tr>
<th>FEC Type</th>
<th>Average bit errors corrected</th>
</tr>
</thead>
<tbody>
<tr>
<td>BCH (Hard Decision)</td>
<td>70</td>
</tr>
<tr>
<td>LDPC Hard Decision Decoding</td>
<td>75</td>
</tr>
<tr>
<td>LDPC Soft Decision Decoding</td>
<td>265</td>
</tr>
</tbody>
</table>

*Codeword length = 1K User Bytes + 10.7% parity for all three FECs
LDPC Implementation

- Single LDPC instance for easy integration
- Achieve 400 MHz on 7 series and UltraScale™ FPGAs
- Small footprint – low LUT counts
Hardware Reference Board

- Custom made NAND FMC daughter card
- Work with Kintex® UltraScale KCU105 board
  - XCKU040-2FFVA1156E FPGA
- NAND characterization and hardware validation
Summary

- Xilinx offers LDPC with industry-leading performance in all aspects:
  - Error floor
  - Resource utilization
  - BER performance
  - Throughput