High Performance, FPGA-Optimized LDPC for Storage

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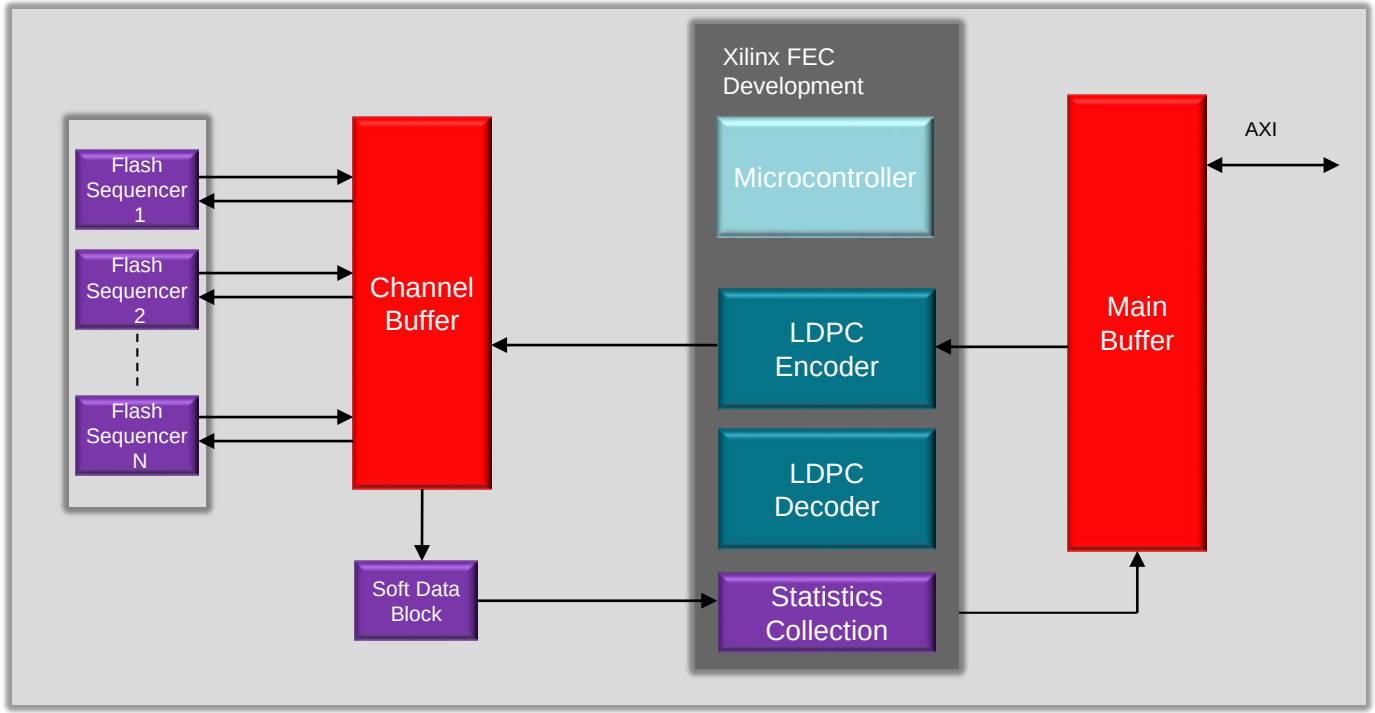
LDPC and Error Correcting Codes

- **BCH codes are running out of steam**
  - Can't take advantage of soft-data
  - Performance is limited to the Shannon limit for a hard channel
- **LDPC codes**
  - Near Shannon-limit performance
  - Take advantage of soft-data
  - Good implementations of LDPC codes are low power and cost effective
- **No standards for LDPC in storage space**
- **Code "growth" technology with best-in-class coding performance at very low cost**

Sub-system block diagram

- **DSP work is focused on the LDPC encoder, decoder and statistics processing below**



Xilinx LDPC Features

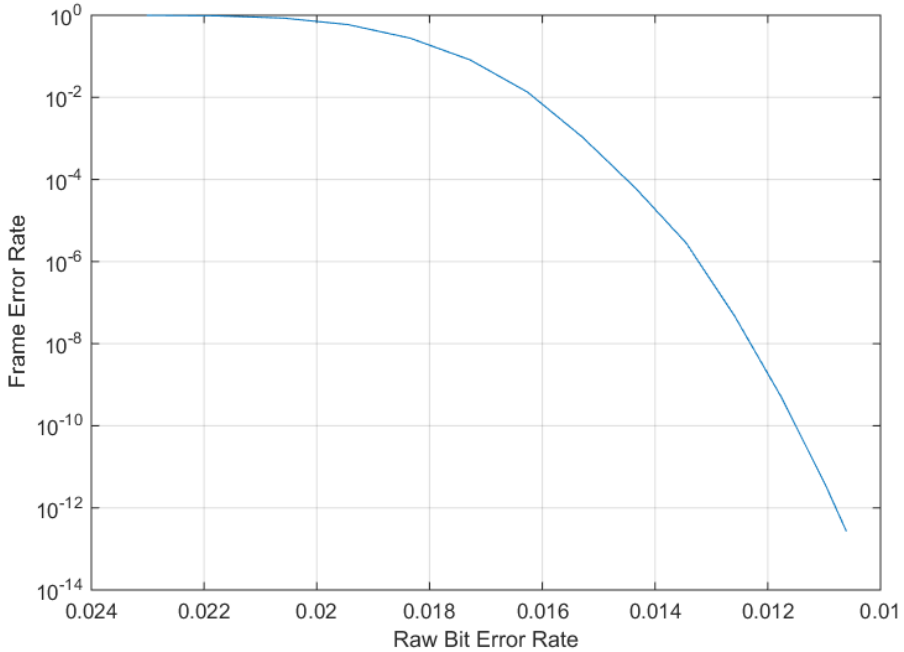
- Best-in-class code performance near Shannon limit
- Achieved low error floor under 10^{-15} with proprietary optimization method
- Support for code rate change on-the-fly
- Support both hard decision and soft decision decoding
- High throughput and low latency performance
- Scalable architecture supporting various options
- FPGA optimized for minimal area/power
- Provides decoder status and statistics interfaces

Xilinx LDPC Specifications

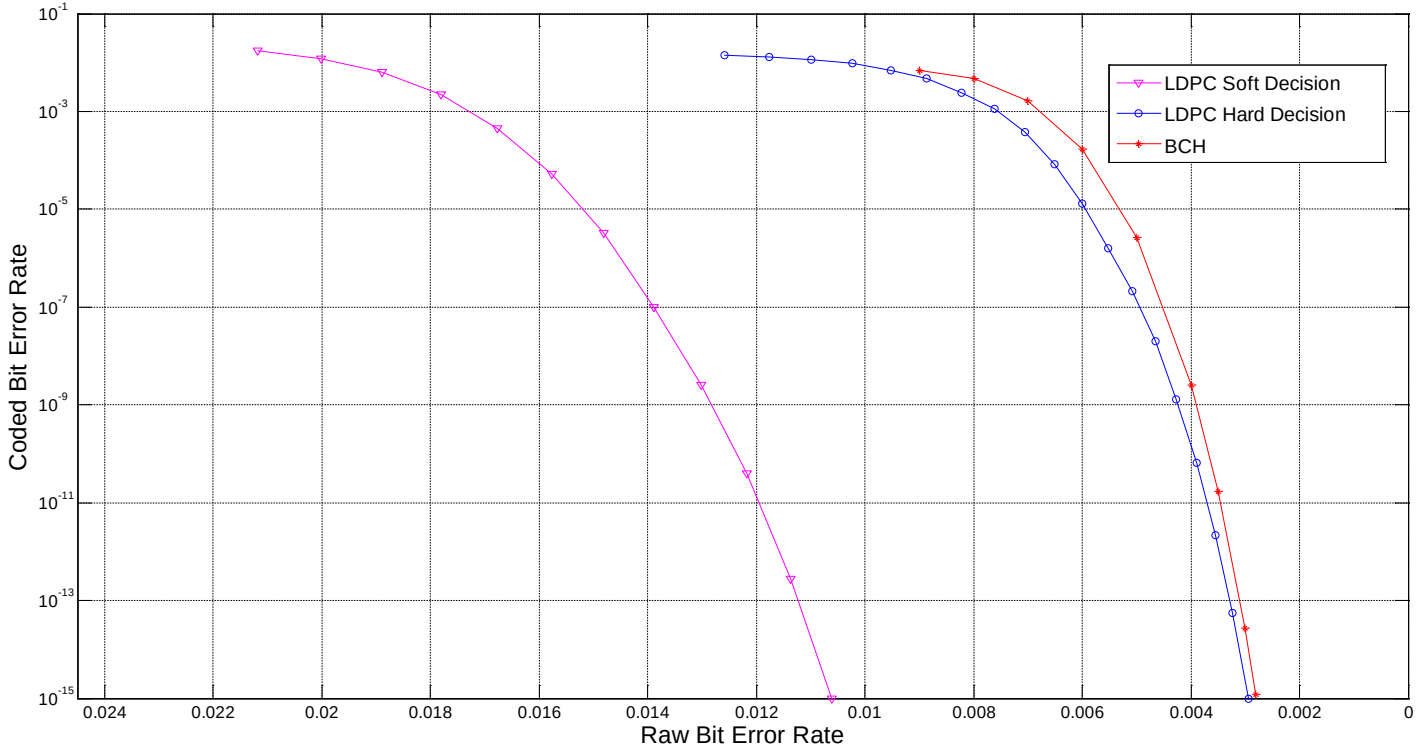
Feature	Specification
Codeword Length	1K Bytes + parity
Code Rate	Various options above .89
Rate switching on-the-fly	☑
Error Floor	Better than 10^{-15}
Two Step Decoding	☑
Early Termination	☑
Device Supported	Ultrascale, 7-series
Clock Rate	400MHz

Raw BER v.s. Frame Error Rate

- **Advanced code construction methodology for best code performance**
- **Achieved low error floor using proprietary optimization technique**
- **Near Shannon limit performance**

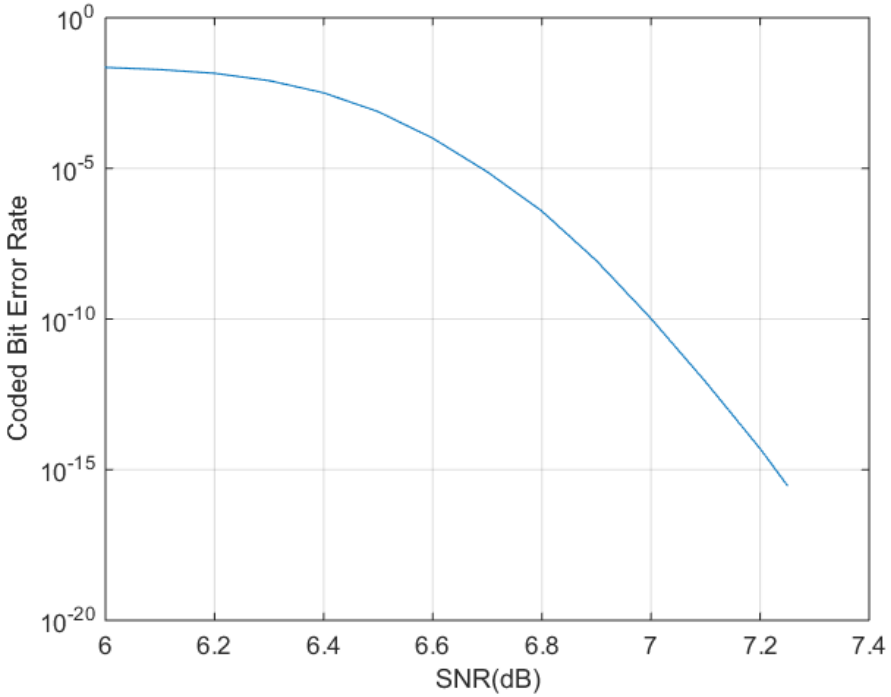


LDPC v.s. BCH Performance



- **Codeword length = 1K User Bytes + 10.7% parity**
- **BCH: T=70**

Error Floor Free Performance



Error Correction Capability

- >3x Average Bit Errors Corrected using LDPC Soft Decision Decoding

FEC Type	Average bit errors corrected
BCH (Hard Decision)	70
LDPC Hard Decision Decoding	75
LDPC Soft Decision Decoding	265

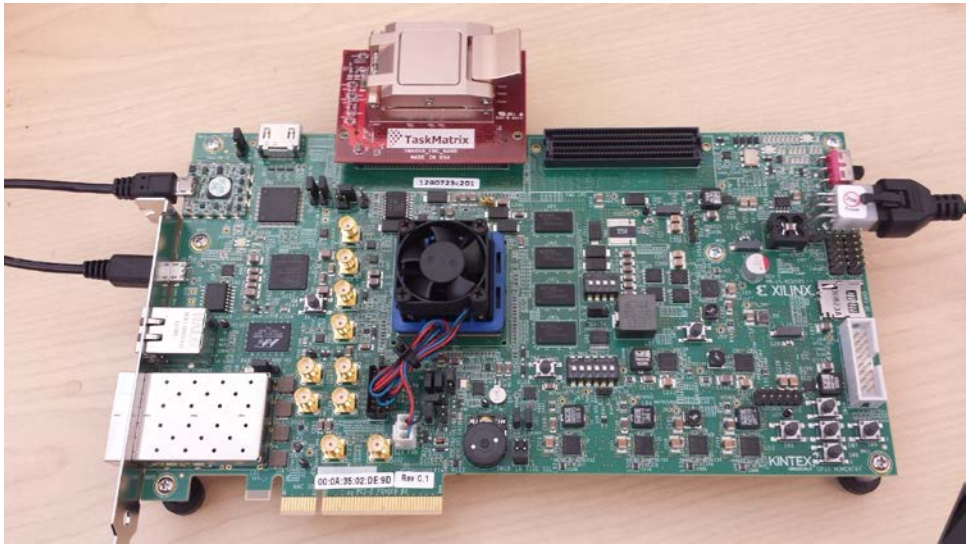
***Codeword length = 1K User Bytes + 10.7% parity for all three FECs**

LDPC Implementation

- Single LDPC instance for easy integration
- Achieve 400 MHz on 7 series and UltraScale™ FPGAs
- Small footprint – low LUT counts

Hardware Reference Board

- **Custom made NAND FMC daughter card**
- **Work with Kintex® UltraScale KCU105 board**
  - XCKU040-2FFVA1156E FPGA
- **NAND characterization and hardware validation**



Summary

- **Xilinx offers LDPC with industry-leading performance in all aspects:**
  - Error floor
  - Resource utilization
  - BER performance
  - Throughput