Scalable Flash Architectures Meet “Instant On”

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Explosion of More Intelligent and Connected Devices

In 2013, there were 23M connected cars. In 2015, 20% of vehicles sold will be connected. By 2020, there will be 152M connected cars sold globally.  Source: IHS
Explosion of Connected Autos

Cypress + Spansion = No. 3 in Automotive Memory & MCUs

- **Chassis**
  - Power Steering
  - Antilock Brake
  - Steering Sensor
  - Stability Control

- **Safety/ADAS**
  - TPMS
  - Air bag
  - Telematics
  - Rearview Camera
  - Multi-Camera

- **Body Electronics**
  - Body Control
  - Gateway Control
  - Wiper
  - Window
  - Lights
  - Mirror
  - Seats
  - Doors

- **Infotainment**
  - Head-up Display
  - Instrument Cluster
  - GPS and Navigation
  - Satellite Radio
  - Blue-ray/DVD
  - Audio Systems
  - Central Information Display
  - Rear-Seat Entertainment

- **Driver Information**

- **Voice Recognition**
- **Touch and Character Recognition**
- **Climate Control / HVAC**
  - Fuel Injection
  - Motor Control Unit (HV/EV)
  - Battery Charging Control (HV/EV)
  - DCDC Control (HV/EV)
  - Alternator

Flash Memory Summit 2015, Santa Clara, CA
High Performance Automotive Requirements

- TFT replacing mechanical
  Instant on

- Traditional architecture insufficient
  Fast boot
  Graphics recall

- Larger screen and higher resolution
  Complex graphics
  Motion graphics
  More instant on functionality

- Flash NOR Flash for
  Boot, Code, and Graphics

Auto-Cluster

Infotainment
Cypress HyperBus™: A Better Solution

HyperBus™ Interface
A high-bandwidth, 12-signal interface that transfers information over 8 I/O signals at double data rate (DDR), delivering up to 333 MBps

HyperFlash™ NOR Flash Memory combines the industry’s **highest Read Bandwidth**...

With one of the **lowest-pin-counts available**...

HyperBus™ Interface (12 pins)

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**Read Bandwidth (MBps)**

<table>
<thead>
<tr>
<th></th>
<th>Hyper-Flash</th>
<th>DDR Quad</th>
<th>SPI</th>
<th>Page Mode Parallel</th>
</tr>
</thead>
<tbody>
<tr>
<td>350 MBps</td>
<td></td>
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<tr>
<td>300 MBps</td>
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<tr>
<td>250 MBps</td>
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<td></td>
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<tr>
<td>200 MBps</td>
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<tr>
<td>150 MBps</td>
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<td></td>
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</tr>
<tr>
<td>100 MBps</td>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>50 MBps</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0 MBps</td>
<td></td>
<td></td>
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</tr>
</tbody>
</table>

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**Pins for Data Transfer (# of Pins)**

<table>
<thead>
<tr>
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<th>Hyper-Flash</th>
<th>DDR Quad</th>
<th>SPI</th>
<th>Page Mode Parallel</th>
</tr>
</thead>
<tbody>
<tr>
<td>50 pins</td>
<td></td>
<td></td>
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<td></td>
</tr>
<tr>
<td>45 pins</td>
<td></td>
<td></td>
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<tr>
<td>40 pins</td>
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<td></td>
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<tr>
<td>35 pins</td>
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<tr>
<td>30 pins</td>
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<tr>
<td>25 pins</td>
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<td></td>
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</tr>
<tr>
<td>20 pins</td>
<td></td>
<td></td>
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<td></td>
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<tr>
<td>15 pins</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>10 pins</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5 pins</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0 pins</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

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**HyperBus™ Interface**
A high-bandwidth, 12-signal interface that transfers information over 8 I/O signals at double data rate (DDR), delivering up to 333 MBps
**HyperBus™ and HyperFlash™ Memory**

Industry’s fastest NOR Flash Memory for the highest-performance systems

<table>
<thead>
<tr>
<th>Problems Designers Face</th>
<th>HyperFlash™ Solves These By:</th>
</tr>
</thead>
<tbody>
<tr>
<td>The highest-performance systems for fast boot with graphics display</td>
<td>A DDR mode with up to 166-MHz with 333-MBps Read Bandwidth</td>
</tr>
<tr>
<td>Low-pin-count interfaces to reduce system cost</td>
<td>A standard 24-ball package sharing a common footprint with Quad SPI and Dual Quad SPI simplifies board layout</td>
</tr>
<tr>
<td>They must have high system reliability</td>
<td>On-chip ECC to provide a FIT rate &lt;0.1 FIT per device</td>
</tr>
<tr>
<td>High temperature ranges</td>
<td>An extended operating temperature range of -40°C to +125°C</td>
</tr>
</tbody>
</table>

To enable demanding high-performance systems

**Example:**
Automotive Instrument Cluster
# HyperFlash™ vs. Traditional Flash

<table>
<thead>
<tr>
<th>Feature</th>
<th>S26KS Family</th>
<th>2 x S25FS Family</th>
<th>S25FS Family</th>
<th>SPI</th>
</tr>
</thead>
<tbody>
<tr>
<td>Interface</td>
<td>HyperBus</td>
<td>2 x Quad SPI</td>
<td>Quad SPI</td>
<td>Quad SPI</td>
</tr>
<tr>
<td>I/O Pin Count</td>
<td>8</td>
<td>8</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>Clock Rate (DDR)</td>
<td>166 MHz</td>
<td>80 MHz</td>
<td>80 MHz</td>
<td>54 - 66 MHz</td>
</tr>
<tr>
<td>Read DDR Bandwidth (max)</td>
<td>333 MBps</td>
<td>160 MBps</td>
<td>80 MBps¹</td>
<td>54 - 66 MBps¹</td>
</tr>
<tr>
<td>Program Time (512B)²</td>
<td>0.475 ms</td>
<td>0.475 ms</td>
<td>0.475 ms</td>
<td>1.0 ms³</td>
</tr>
<tr>
<td>Sector Erase Time (256KB)²</td>
<td>930 ms</td>
<td>930 ms</td>
<td>930 ms</td>
<td>1400 ms⁴</td>
</tr>
<tr>
<td>Chip Erase Time²</td>
<td>110 s</td>
<td>120 s</td>
<td>120 s</td>
<td>240 s</td>
</tr>
<tr>
<td>Temperature Range</td>
<td>-40°C to +125°C</td>
<td>-40°C to +105°C</td>
<td>-40°C to +105°C</td>
<td>-40°C to +85°C</td>
</tr>
</tbody>
</table>

1. Calculated using DDR clock rate
2. Conditions: 25°C and \( V_{DD} \) 3.0 V, 100k minimum endurance
3. Parts do not support 512B Programming. Program time is calculated using two 256B Program operations.
4. Parts do not support 256KB Sector Erase. Erase time is calculated using four 64KB Sector Erase operations.

## Competitive Comparison

- **Faster Boot, Bigger Display, Higher Resolution, Fancier Graphics, Smoother Motion**
Other Implications for High Performance Flash

- Fast Initial Access
- High Sustained Read Throughput
- Cypress HyperRAM™ serves as a companion RAM
  - Reduced controller pin count
  - Simplified PCB layout
  - Space-saving packaging

HyperFlash™ Memory
- Performance
- Low Pin Count
- Low Systems Cost

Parallel & SPI NOR

Reduce or Eliminate DRAM

Flash-less SoC or Additional Flash

Embedded Flash in SoCs/MCUs

Alternative to Traditional NOR