An FPGA Based Enterprise SSD Reference Design

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“The IP enabled solutions provider”
AGENDA

FPGA Based Enterprise SSDC

Design Challenges

Configurable IP Components

Mobiveil SSDC Reference Design

Summary
FPGA Based NVMe Enterprise SSDC Reference Design
NVMe Based Enterprise SSDC

Device FW

ARM Cortex A9  
GPIO  
DDR3/4 Controller

HPS

PCle PHY  
PCle HIP  
NVMe Controller  
Enterprise Flash Controller

On Chip Data Path
On Chip Control Path
Inter block Interconnect

Design Challenges
Configurable IP Components
Mobiveil SSDC Reference Design
Summary

FPGA Based Enterprise SSDC

HPS

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Design Challenges

- Reference Design should be flexible to support different hardware configurations
- Reference Design should be able to handle various target technologies
  - It should be able to handle performance targets across technologies
- Reference Design should allow customization for individual implementations
- Reference Design should provide hooks for Statistics gathering, Error recovery, Reclaim and other value added Enterprise SSD functions
Feature Configurability

- FPGA Based Enterprise SSDC
- Design Challenges
- Configurable IP Components
- Mobiveil SSDC Reference Design
- Summary

- Error Correction
  - LDPC/BCH
- Number of IO Queues & Depth
- Vendor Defined Commands
- Flash Endurance Support
- Vendor Specific Command Arbitration
- Number of Flash Channels
- Flash Interface Type
  - Toggle/ONFI
- Multi-Path IO Support
Implementation Challenges

- Efficient Buffering
- Data Path Width Support
- Number of DMA Engines
- Interfacing with 3rd Party VIPs
- Interfacing with 3rd Party IPs
- Processor Dependent ??
- Clock Frequency
- HW/SW Partitioning

FPGA Based Enterprise SSDC
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Summary
Configurable NVMe Based SSDC

Design Challenges
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Summary

Address all Features
Design, Implementation, Verification Effort
Area, Frequency
Latency, Bandwidth, QOS

FPGA Based Enterprise SSDC
Configurable IP Components
UnH Certified NVM Express Controller IP (UNEX)
NVM Express (UNEX) Controller

- Highly Configurable
- Technology Independent

UNH Certified

Design Challenges
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Summary

FPGA Based Enterprise SSDC

Agenda
PCI Express Controller (GPEX)
FPGA Based Enterprise SSDC

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Summary

PCI Express (GPEX)

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Design Challenges

Configurable IP Components

Gen1, Gen2 & Gen3 Endpoint
Root Complex
Dual mode
Switch port
Switch
OCB Solution
x1 to x32
180nm to 28nm

Application Interface

Trans Layer
Link Layer
MAC Layer

Logics Layers

PHY Layers

TRX
TCTL
TTX
DRX
DCTL
DTX
MRX
MCTL
MTX

Receive
Control
Transmit

PIPE

Serial

PCS
PMA

Flash Memory SUMMIT

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FPGA Based Enterprise SSDC

PCle-AMBA Bridge

Design Challenges

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Summary

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Design Challenges

Configurable IP Components

Summary
DDR3/4 Memory Controller
DDR3/4 Controller Requirements

- Compliant with AXI4
- Compliant with DFI 3.1 Interface
- Supports QoS through various arbitration schemes
- Configurable and programmable address mapping
- Supports up to 4 ranks
- Supports following BC Clock to PHY Clock ratio
  - 1:1 (Full-rate Mode)
  - 1:2 (Half-rate Mode)
  - 1:4 (Quarter rate Mode)
- Supports Burst Length 4, 8, 16
- Supports Active/Precharge Power down
- Supports software and hardware driven Self Refresh entry and exit
- Supports Auto-refresh and per-bank refresh
- Supports ECC Checking and Correction (optional)
- Supports automated memory initialization
- Supports ZQ Calibration
DDR3/4 Memory Controller

**Agenda**

- Highly Configurable
- Technology Independent

**Design Challenges**

- Configurable IP Components
- Mobiveil SSDC Reference Design

**Summary**

- Highly Configurable
- Technology Independent
Enterprise Flash Controller
Enterprise Flash Controller

- Highly Configurable
- Technology Independent

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FPGA Based Enterprise SSDC

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Enterprise Flash Controller

- Memory IF
- Control Path IF

HCA

HIF

FIMA

FC

FC0

Flash IF

Data Path IF

Agenda

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Enterprise Flash Controller Requirements

- **Hardware Command Accelerator**
  - FTL in Hardware
  - Manages all Flash Translation Tables
  - Provides Interface to Device FW for Reclaim, Flash endurance Error Logging and other diagnostic feature implementation

- **Flash Interface and Media Access**
  - Temporal Sequencing of Read/Write Commands to obtain maximum performance
  - Striping and De-striping of data between multiple flash channels (Scatter/Gather).
  - Computation and Checking of Raid Parity
  - Manage the Usage Pools of data (like Hot/Cold Data)
  - Implements ECC
  - Implements Encryption/Decryption
  - Implements Compression/Decompression
Enterprise Flash Controller Requirements

- **Host Interface**
  - Interfaces with NVMe controller Datapath

- **Flash Controller**
  - Implements Flash Interface State Machine
NVMe Based Enterprise SSDC

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FPGA Based Enterprise SSDC

ARM Cortex A9
GPIO
DDR3/4 Controller

Device FW

On Chip Data Path
On Chip Control Path
Inter block Interconnect

Certified IP

Certified IP from Mobiveil

PCIe PHY
PCle IP*
NVMe Controller*
Enterprise Flash Controller

Flash
DDR3/4

Configurable IP Components

Mobiveil SSDC Reference Design
Summary

FPGA Based Enterprise SSDC
Functions & Configurability

- Highest Performance SSD Reference Design with TLC NAND Technology
- UNEX (Universal NVM Express controller) compliant to NVMe 1.2 specifications
- Up to 16 channels of NAND flash array
- Offers up to 4TB Capacity
- Available as M.2/3.5inch form factor drive or PCIe Add-in card form factor (Half-height and Half-length)
- Rigorous Qualification and JEDEC JESD218A compatibility testing ensures high reliability
The Mobiveil Team

• Leadership
  – Management with 25+ years experience in Semiconductor/Silicon IP/Systems software
  – Previously founded GDA Technologies, Inc and grew to strong IP and Services group, 500+ engineers strong

Key differentiators

Developed several highly configurable key high speed IP blocks in the last 10+ years (PCI Express, Hyper Transport, Serial RapidIO, SPI4.2, DDR4/3, NVMe and Enterprise Flash Controllers)

Locations

Headquarters in Milpitas, CA
India design centers: Chennai & Bangalore
Sales: Offices/Reps worldwide
Mobiveil IP Advantages

- Market leading & most exhaustively proven cores in the market: Industry leaders are using these cores
- Consortium Participation: RIO – Member, PCISIG – Member, HMC - Member
- Superior Technical Solution: Most Feature rich IP, Complete Customization and delivery Solution
- Support: Clear IP Focus & Worldwide Support
- 3rd Party Partnerships for complete Solution: (Verification and PHY IPs)
- Standard Body Certified Cores: All Mobiveil IPs are validated and certified: PCI Plug fest, UNH, RTA
Thank you.

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