

Building a Controller That Can Handle Any Type of Flash

Brent Przybus – Sr. Director eASIC Corporation





A Changing Flash Enabled Landscape

- Flash Is Needed for Enterprise Storage
- Flash is Evolving Rapidly Due to Demand
- The Controller Architecture Must Evolve



Expanding Role of Flash in Enterprise Storage

- Application and Data Velocity is Increasing Exponentially
 - Flash based storage is faster than disk
 - But this speed is not needed across the spectrum
- Flash is More Reliable Than Ever
 - Suitable for broad use in the data center
 - Provided you are using the right controller

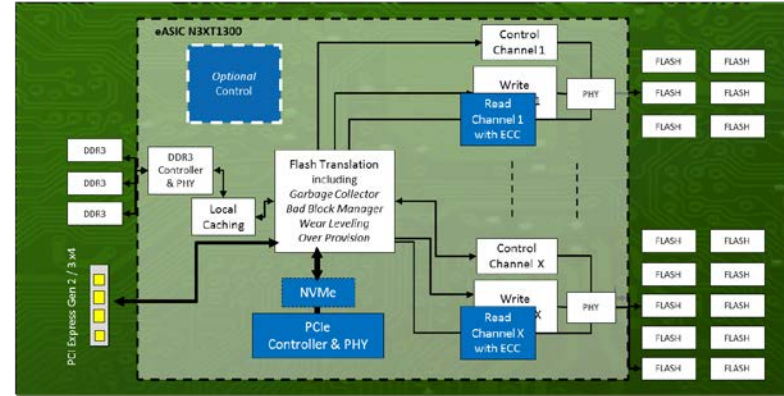
Redefining the Boundaries

- Transitioning to Scale-out Architecture
 - Better suited for data centers
 - Better support for different data types
- Opportunity to Redefine the Controller
 - Support flexible hardware / software partitioning
 - Support for virtualization



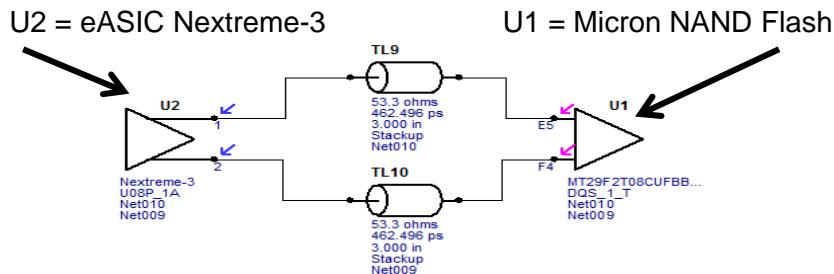
Anatomy of the Ideal Controller

- Low Power
 - <5 Watts
- Flash Memory Interface Speed
 - ONFI 4 800MT/s, Multiple instances
- Host side Flexibility
 - PCIe Gen3 x8/16 or SAS/SATA or Ethernet...
- Fast, Flexible FTL Memory
 - DDR4, DDR3, LPDDR, etc.
- Flexible Processor Support
 - FTL Control and Management
- Efficient ECC
 - Multiple Instances of BCH or LDPC
- Independent Channel Support
 - Flexible Multiple Channel DMA Support



eASIC Nextreme-3 ONFI Support

Capability	ONFI Requirement	eASIC Nextreme-3 eIO Spec
Signaling Standard	1.2V/1.8V SSTL	✓
Data rates (MT/s)		
ONFI 3.0/3.2	400, 533	✓
ONFI 4.0	667, 800	✓
ZQ Calibration		
Driver impedance (ohms)	25, 35, 50	✓
ODT (ohms)	50, 75, 100, 150	✓
I/O Leakage Currents (uA)	+/- 10	✓

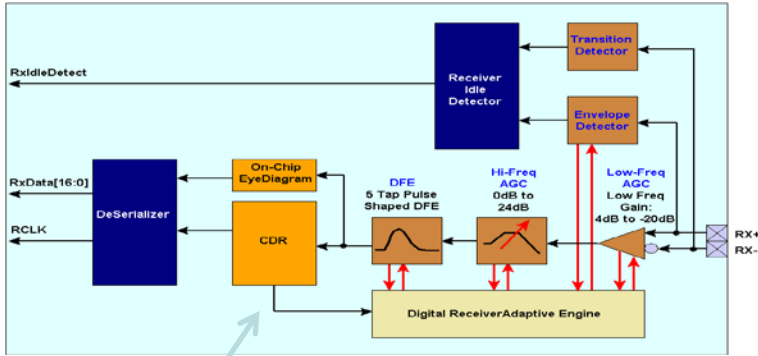


Data Rate	Load Count	Operation
533 MT/s	16	Read/Write ✓
667 MT/s	8	Read/Write ✓
800 MT/s	8	Read/Write ✓

eASIC Nextreme-3 eIO NV-DDR3 Load Analysis



eASIC MGIO PCIe with SRIS

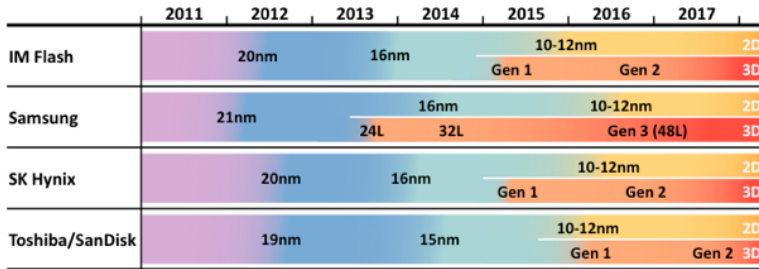


Requirement	SRIS Requirement	MGIO Spec
Clock tolerance capability (ppm)	5600	5600
RX-CDR PLL (Type; BW)		
Gen-2	2 nd order; 5 MHz	2 nd order; 5 MHz
Gen-3	2 nd order; 10 MHz	2 nd order; 10 MHz
PCS (Elastic Buffer) Req.		
Gen-2	1 SO-set* / 154 symbols	Supported
Gen-3	1 SO-set* / 38 symbols	Supported

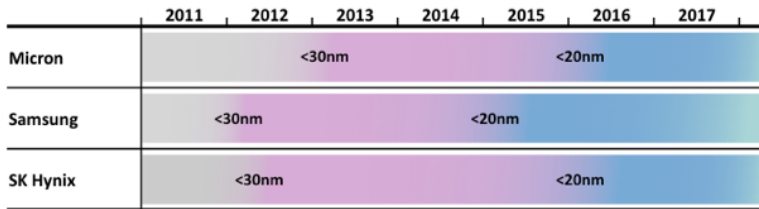
- RX-CDR implemented with fully independent PLL (2nd order high-pass function)
 - Allows much faster tracking of phase variation on incoming data
 - Meets the 5600 ppm SRIS-required spread-spectrum tracking capability

The Evolution of Flash

NAND Flash Process Roadmaps (for Volume Production)



DRAM Process Roadmaps (for Volume Production)



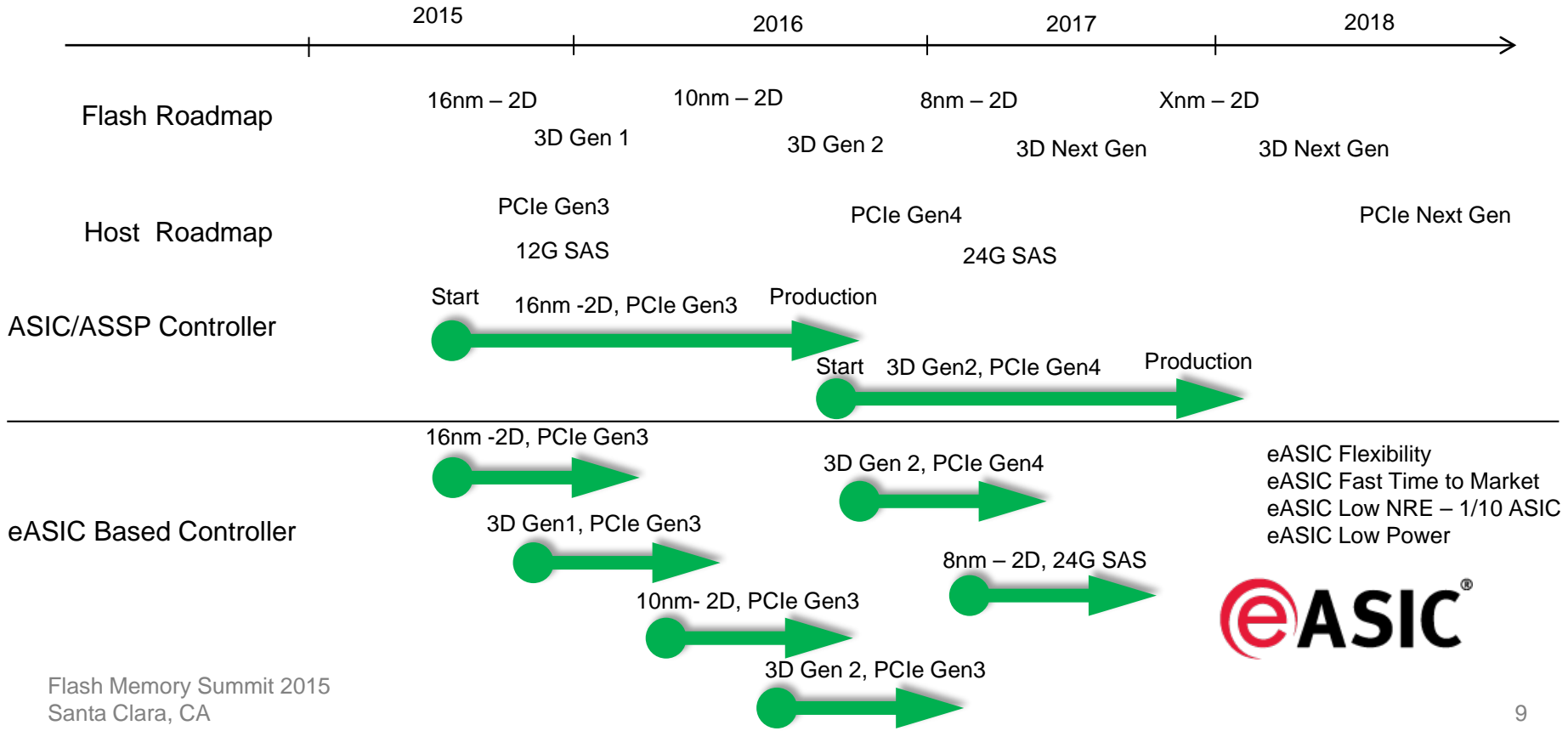
Note: What defines a process "generation" and the start of "volume" production varies from company to company, and may be influenced by marketing embellishments, so these points of transition should be used only as very general guidelines.

Sources: Companies, conference reports, IC Insights

- Flash Controller Trend
 - Constant Change
 - Faster/Lower Latency
 - Faster, Denser, Cheaper

<http://evertiq.com/design/35204>

Avoiding Obsolescence



Comparing Controller Options

Requirements	FPGA	ASIC/ASSP	eASIC Platform
Host Side Flexibility	Any Host	Fixed Interface	Any Host
Flash Interface	Flexible	Fixed	ONFI 4 at 800MT/s
Power Consumption	12 Watts	2 Watts	5 Watts
Ability to Customize	Yes	No	Yes
Time to Market	RTL to Proto – Very Short	12 + Months	RTL to Proto – 7 weeks
DDR Memory Speeds	DDR4 2.6Gbps	Fixed	DDR4 2.1Gbps DDR3 2.1Gbps
Development Cost	No NRE	Millions in NRE	1/10 ASIC NRE
Unit Price	Highest	Lowest	Low



Top 5 Things to Ask About Your Controller Architecture

1. Does it support the latest Flash technology.... Will it keep up?
2. Are your competitors using the same controller?
3. Does it deliver the performance per watt you need?
4. Does the same controller multiple host interfaces?
5. How fast is the Flash interface?

- Flash is Changing Storage
- Flash is Evolving Fast to Deliver More
- You Need a Flexible Controller that Keeps Up