



**avalanche**technology

*Spin Programmable Storage Solutions*

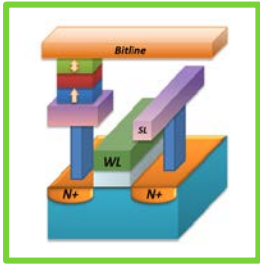
# pMTJ Driven STT-MRAM Sampling From 300 mm Process

Avalanche Technology Inc.

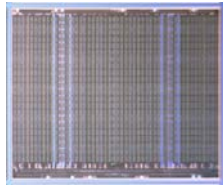
Yiming Huai  
VP of Technology

# Avalanche Technology — at a Glance

Avalanche  
Proprietary  
STT MRAM  
Technology



Stand-alone **SPMEM™**



Avalanche 64 Mb chip

Embedded **AvRAM™**



Large Markets



Enterprise Storage, Mobile,  
Telecom & Computing (SAM \$15B)

Founded in 2006

*Led by an Experienced Team*



Industry Veterans Delivering  
Innovative Storage Solutions

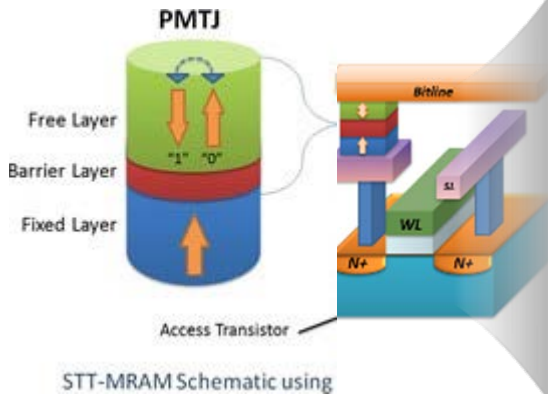
*Supported by extensive patent  
portfolio*

240+ patents filed  
with 165+ granted /allowed

*Backed by Top Tier VCs*



# AVA pMTJ: Enabling STT MRAM Towards Mainstream Memory

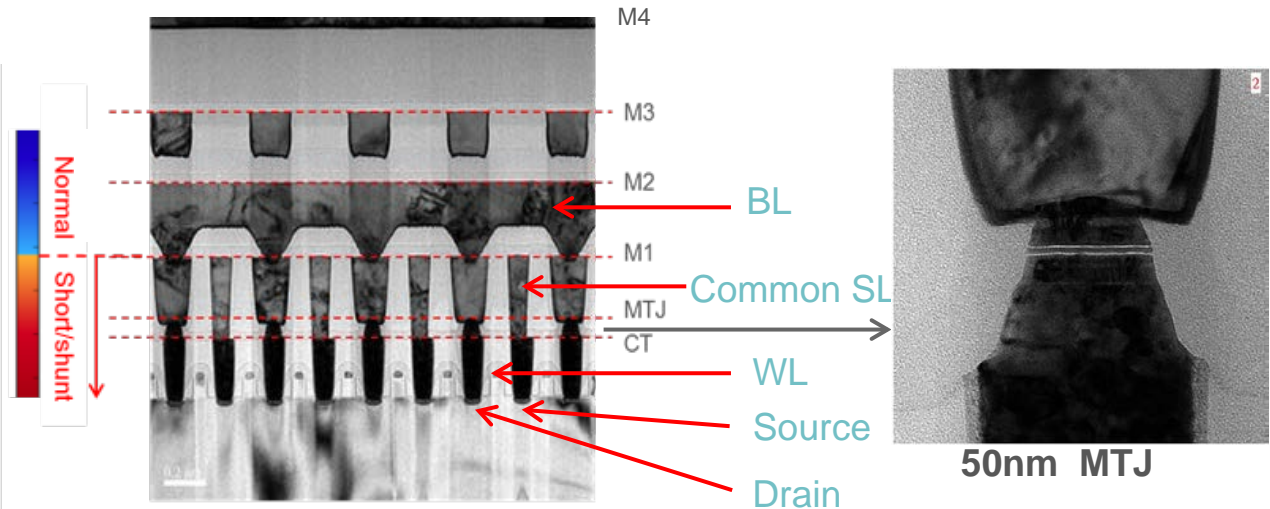
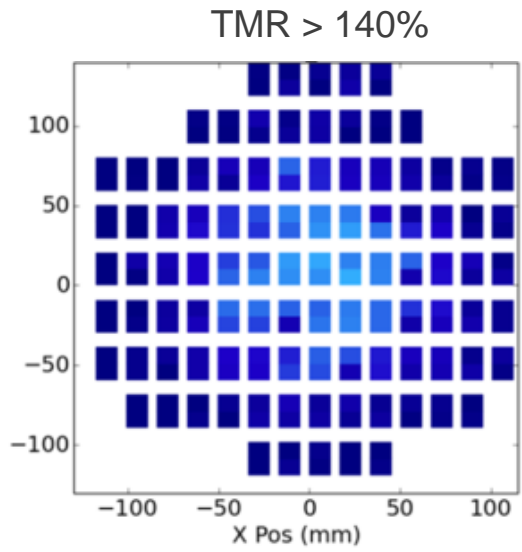


- Highly scalable to 1x nm: low write current ( $<100 \mu\text{A}/350\text{mV}$ ) with sustainable high thermal stability  $\Delta > 80$
- Excellent write performance (sub ns and low WER  $< 10^{-8}$ )
- High TMR  $\sim 200\%$  (targeting 250 % in near future)
- Thermally stable TMR up to  $400 \text{ }^\circ\text{C} > 60 \text{ min.}$   
→ compatible with standard CMOS (embedded)
- High Endurance  $> 10^{16}$  cycles
- Excellent Manufacturability ( $< 1\text{x nm}$ ): thin stack  $< 200\text{A}$

AVA pMTJ delivered all attributes required for a disruptive non volatile memory

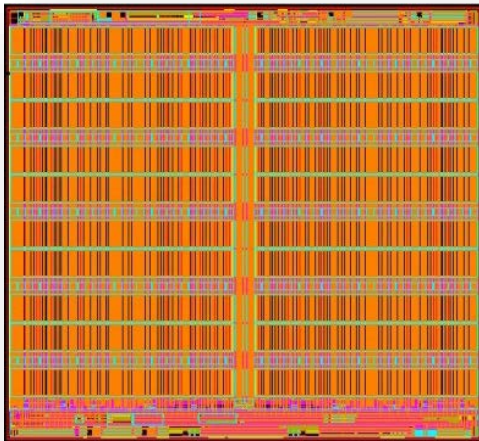
# Avalanche Advanced 300 mm BEOL Integration

- Advanced LP CMOS (40-50 nm) in world-class foundry
- Low cost adder with single MTJ etch mask
- Scalable (<1nm) MTJ BEOL integration process flow (portable to other foundry)
- TMR thermally stable up to 400 °C, compatible with embedded applications.
  - **Note – MTJ below M1 as shown. Portable between any 2 metal layers.**



## Avalanche Industry's First pMTJ 55nm SPI 64/32 Mb Chip: Customer Sampling Stage

- Write/Read Speed < 50 ns
- BER < 10<sup>-8</sup>
- Data Retention > 10 Years
- BEOL: Cu, 4 Metal Layers
- Endurance: ~10<sup>16</sup>



CS#	1	8	VDD
DQ1/ SO	2	7	DQ3/ HOLD#
DQ2/ WP#	3	6	SCK
VSS	4	5	DQ0/ SI

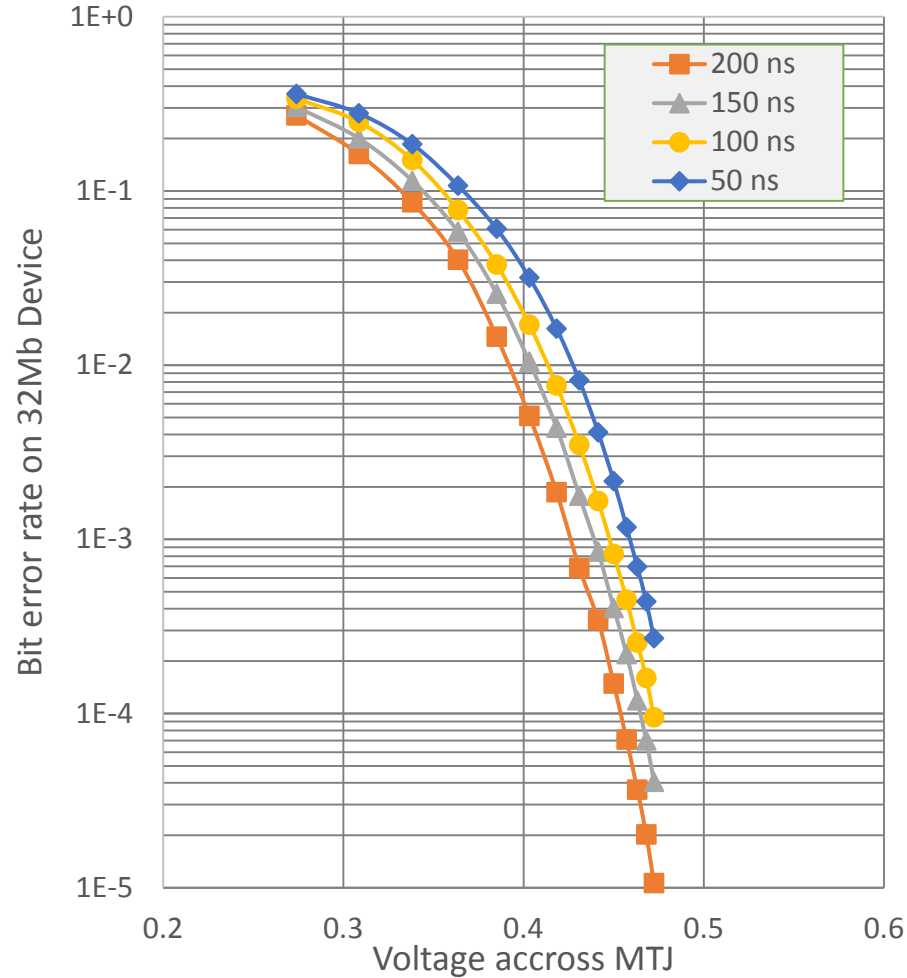
### Basic Features:

- Single Power Supply Operation  
1.65V – 1.95V Read and Write Operations
- Serial Interface Architecture  
SPI Compatible: Mode 0 and Mode 3
- 32/64M-bit Density  
Uniform 256-byte Page  
Uniform 4K-byte Sector  
Uniform 64K-byte Block
- Performance Driven: 108MHz Clock Frequency (13.5MB/s)
- Quad Output Fast Read & Quad I/O Fast Read @54MHz  
Clock Frequency (27MB/s)
- Low Power Consumption
- Package: 8-Pin WSON

**64 Mb chip with Industry Standard SPI fabricated with 55 nm LP CMOS  
at world class foundry**

# Write Shmoo (No ECC and No Redundancy)

BER plot- 99.99% yield



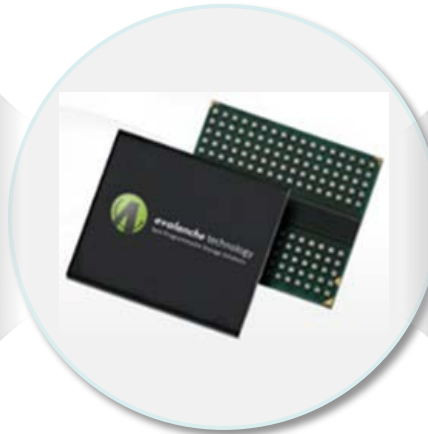
# Avalanche STT-MRAM: Revolutionizing System Design for a Wide Range of Applications

## Stand Alone Solutions

- Memory buffers
  - Persistent DRAM
- Battery backup SRAM
- DRAM
- New Market Applications
  - Storage class memory (L4)

## Embedded Solutions

- eNVM
  - eFlash, eOTP, eFuse
- Cache Memory
  - L3, L2..
- eDRAM
- New Market Applications
  - Low standby-power connectivity systems (IoT, wearable electronics)



Avalanche STT- MRAM

- **Low power consumption**
- **Low manufacturing cost**





Thank You!

Visit us at:  
[www.Avalanche-technology.com](http://www.Avalanche-technology.com)