Radiation Effects in SSDs

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IROC Technologies
Outline

- Introduction
- Soft Errors in SSDs
- Radiation Testing
- Test Results
- Early Reliability Analysis
- Conclusion
Introduction
Soft Errors are caused by ionizing radiations (neutrons, alpha particles)

- Interaction with silicon
- Charge deposition and collection
- Current spike
- Upset (SEU) or Transient (SET)
Source of Ionizing Radiation

- Neutrons (High energy and Thermal) generated by high energy particles, coming from space, entering the atmosphere and interacting with the air (Nitrogen, Oxygen, …)

- Alpha particles generated by traces of radioactive materials in the packaging materials
Soft Error Trend

- **Voltage Effect**
  - Lower voltage $\rightarrow$ increased sensitivity

- **Smaller devices**
  - Lower target area $\rightarrow$ reduced sensitivity
  - Smaller stored charge $\rightarrow$ increased sensitivity

- **Number of devices (SRAM cells, flip-flops)**
  - More devices $\rightarrow$ increased total sensitivity

- **Transistor type**
  - FINFETs show lower sensitivity than planar transistors

- **Increased awareness**
  - Increased awareness results in more careful design
Soft Errors in SSD
SSD Architecture

Main SSD Components and Risk

<table>
<thead>
<tr>
<th>Component</th>
<th>Type</th>
<th>Potential Risk</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mass memory</td>
<td>NAND Flash</td>
<td>Low sensitivity to SER</td>
</tr>
<tr>
<td>Controller</td>
<td>ASIC with SRAM and FF</td>
<td>Unprotected SRAM, FF: high sensitivity</td>
</tr>
<tr>
<td>Buffer/Cache</td>
<td>DRAM or SRAM</td>
<td>Unprotected SRAM: high sensitivity</td>
</tr>
</tbody>
</table>

**Sensitivity by function**

- **Control path, pointer table**: critical items (an error there might not be recoverable)
- **Data path**: less critical
- **Risky time window**: when data is transferred through the buffer before reaching NAND Flash (read/write)
NAND Flash

- Floating Gate Array: “0” pattern (programmed) is usually more sensitive
- Page Buffer → SEUs
- SEFIs:
  - Program errors: complex algorithm, more logic
  - Erasing errors: simple, apply a bias for a fixed amount of time
  - Read/write errors: block upsets, etc
- Impact on time spent on erasing/programming
- Charge Pumps failures: (program/erase affected)
  - Temporary, during irradiation, p/e fails
  - Permanent, p/e fails
  - Degradation, p/e completes but takes longer

Image taken from Bagatin et al. - Single Event Effects in 1Gbit 90nm NAND Flash Memories under Operating Conditions.pdf
• Modify the charge stored in the cell capacitor
• Upset sense amplifier during access
• Upset various logic/control circuits

Controller

• Functions
  - Error correction (ECC)
  - Wear leveling
  - Bad block mapping
  - Read scrubbing and read disturb management
  - Read and write caching
  - Garbage collection
  - Encryption

Soft Errors affecting the Controller may cause:
device hang, brick and even data corruption
System and chip-level requirements for the maximum acceptable rates of soft errors must be driven by standards (JEDEC JESD218) or customer imposed requirements (Bit Error Rate, QoS, SLA, MTBF ...)

<table>
<thead>
<tr>
<th>Number Deployed SSD</th>
<th>50</th>
<th>100</th>
<th>500</th>
</tr>
</thead>
<tbody>
<tr>
<td>1000</td>
<td>0.036</td>
<td>0.072</td>
<td>0.36</td>
</tr>
<tr>
<td>5000</td>
<td>0.18</td>
<td>0.36</td>
<td>1.8</td>
</tr>
<tr>
<td>10000</td>
<td>0.36</td>
<td>0.72</td>
<td>3.6</td>
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<td>3.6</td>
<td>18</td>
</tr>
<tr>
<td>100000</td>
<td>3.6</td>
<td>7.2</td>
<td>36</td>
</tr>
<tr>
<td>500000</td>
<td>18</td>
<td>36</td>
<td>180</td>
</tr>
<tr>
<td>1000000</td>
<td>36</td>
<td>72</td>
<td>360</td>
</tr>
</tbody>
</table>

Errors per month
Radiation Testing
To evaluate the sensitivity of SSD

- 2 Radiation Test Campaigns were performed at TSL using the ANITA Beam Line (10 SDDs Tested)
- The ANITA beam line reproduces the natural neutron spectrum (neutron energy distribution) but with a higher flux
- Higher Flux → reproduce the effect of thousands of device hours in minutes
Test Setup

To Control Room

Tester  Tester

Power Supply

Shielding (Concrete)

Neutron Beam

SSDs

IROC Golden Device
Test Setup (cont.)

- **SSD Tester**
  - Workstation with Linux operating system
  - SSD accessed as blocks (2048 bits)
  - Allow detection of: brick, hang, flying write, bit errors, ….

- **Golden Device**
  - Measure beam attenuation and alignment

- **Whole device irradiated**
  - Dose effects in DRAM not evaluated
  - Collimated test on controller (next campaign)
Test Results
Device Under Test

10 SSD Tested
• 6 Manufacturers
• 60 to 256 GB
• SATA III Interface
• **Read/Write Error** — error message returned by the kernel
  no data read or written from/in the device

• **Hang** — the device stop working, function resumed after
  power cycle

• **Brick** — the device stop working, function can’t be resumed

• **Silent Error** — error detected by the tester but not reported
  by the kernel
Radiation Test Results

**R/W Error**

![Graph showing R/W Error FIT/Device results]

**Hang**

![Graph showing Hang FIT/Device results]

**Brick**

![Graph showing Brick FIT/Device results]

**Silent Error**

![Graph showing Silent Error FIT/Device results]
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<th>100</th>
<th>500</th>
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</thead>
<tbody>
<tr>
<td>1k</td>
<td>0.0072</td>
<td>0.036</td>
<td>0.072</td>
<td>0.36</td>
</tr>
<tr>
<td>5k</td>
<td>0.036</td>
<td>0.18</td>
<td>0.36</td>
<td>1.8</td>
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</tr>
<tr>
<td>10M</td>
<td>72</td>
<td>360</td>
<td>720</td>
<td>3600</td>
</tr>
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**FIT/SSD**

**ERROR per Month**
Complex Failure Modes

- Persistent failing block (write error)
  - Most of the time fixed after secure erase
- Write operation longer than normal (in some cases lead to a brick)
- Flying write: data written at the wrong location (considered Silent Error)
Early Reliability Analysis
Radiation testing is useful for validation and qualification purposes but...

...requires the device to be manufactured

During the design phase – simulation tools are needed
ASIC Level Analysis

Single Event Effect
- Single Event Transient
- Single Event Upset

Soft Error
- Soft Error in Logic
- SEU in memory = Soft Error

Functional Failure

Flash Memory Summit 2015
Santa Clara, CA
ASIC Level Analysis (cont.)

- Not all SEEs manifest themselves as faults
- Derating factors are significant (often only 1%..10% of SEUs have an observable effect)
- Controller level:
  - TIFT evaluates the sensitivity of the technology
  - SOCFIT accurately calculates derating factors
- SSD level: FMEA approach using database of SER results and experience (and test results)
Reliability Analysis

Example

1000 FIT (raw)

160 FIT (derated)

Fit by Effect
SDC : 15 FIT
DUE : 50 FIT
(NO EFF : 95 FIT)
Simulation Approach

1. Process Response model
   - SPICE NetList
   - Layout GDS2

2. SER Data Base
   - TFIT
   - SoC RTL/Netlist
   - Application

3. Analyzed ASIC design
   - SOCFIT
   - De-rating Analysis
   - Design optimization
Conclusion
Conclusion

- Test results prove the importance of rigorous testing
  - Accurate SER data to integrate in the reliability datasheets and to report to customers
  - Prove successful fulfillment of design targets
    - Standards: JEDEC JESD218
    - Requirements: Bit Error Rate, QoS, SLA, MTBF
  - Suggest recovery actions to improve the overall system reliability
  - Ultimately … discover vulnerable or critical issues before customers do
• Testing needs the manufactured device
  - During the design phase – simulation tools are needed
    ▪ TFIT → Cell level
    ▪ SoCFIT → Chip level
    ▪ FMEA → System level
  - Simulation allows to understand test results
Contact

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Backup Slides
Radiation Test Results

Read/Write Errors (detected)
Radiation Test Results

Hang

![Radiation Test Results Diagram]

Flash Memory Summit 2015
Santa Clara, CA
Radiation Test Results
Brick

![Graph showing FIT/Device vs. Device ID for Brick radiation test results]
Radiation Test Results

Silent Errors

![Graph showing FIT/Device counts for different device IDs (A to J)]