



3D NAND Cost and Transition Timeline

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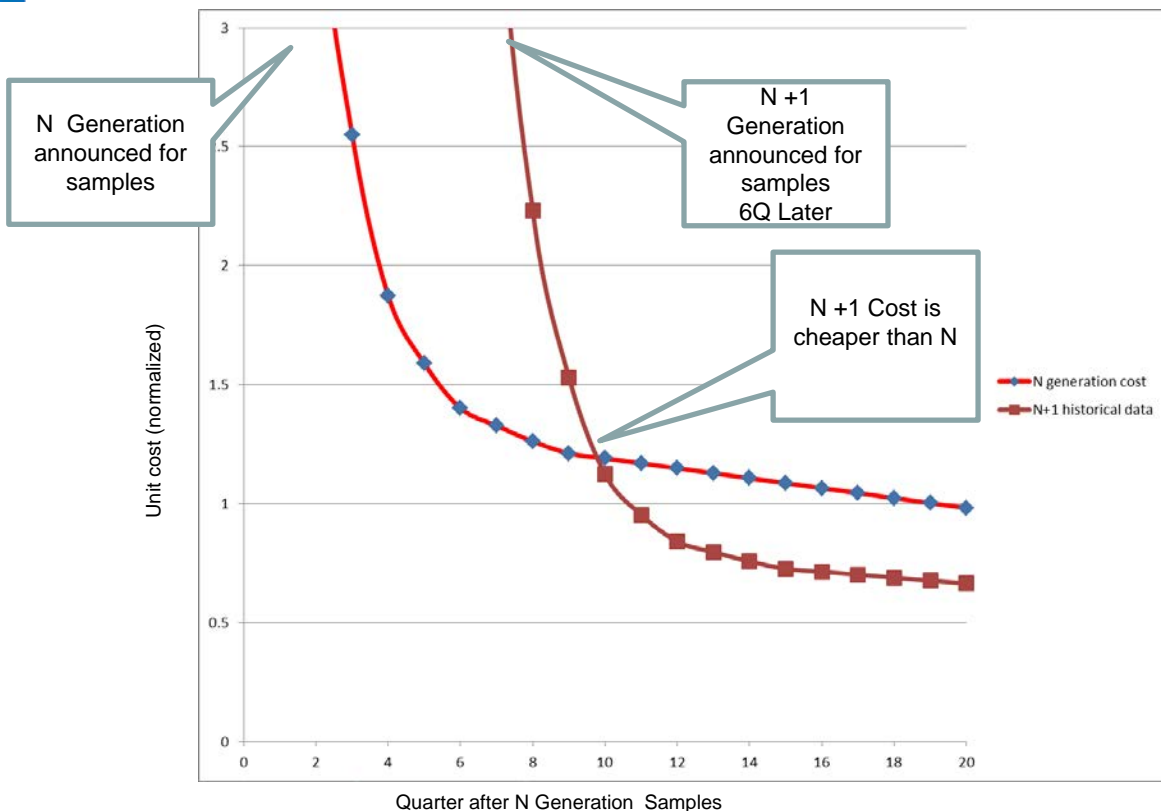
What We Know

- Micron has 128Gb 16nm Planar MLC at 173mm²
- Micron is sampling 32L 256Gb MLC at ~165mm²
- Toshiba has 128Gb 15nm Planar MLC at 139mm²
- Toshiba announced 48L 128Gb MLC and 48L 256Gb TLC
- Samsung is selling 32L, 128Gb TLC with Die size 69mm²
- Samsung has been shipping revenue 3D NAND for over 1 Year
- Samsung is shipping a 16nm Planar die, 64 Gbit MLC at 87mm²
 - Samsung is not just running 3D NAND but 10nm class as well
- Hynix is less clear. They are likely sampling 3D NAND

3D Model/Estimates

- At full production, 32L wafer cost is currently 70% more expensive than 2D NAND
 - Fab output/ft² drops and new equipment needed.
 - 48L is only 5-10% cost adder for 50% more layers.
- Yields are lower for 3D NAND (<50% during initial production)
- Yields approach planar/HVM after >1 Year in production
 - Actual yield is the dominant variable in cost for new technology
- For new technologies, wafer cost and die cost start very high and reduce over lifetime with efficiency and high yields

FMS 2013: ROI on NAND Scaling



Unit cost is very high to start

- High wafer cost
- Low output
- Low yield

Keep improving and new technology wins

Process Technologies

- Samsung NAND process is shipping in volume and has multiple teardowns to show capability and changes over time.
- Geometry terms like 40nm or 20nm are not useful. Architecture is too complex for simple analysis like this.
 - Samsung VNAND was called 40nm. Its actually 20nm or 60nm or 80nm
- Micron device is sampling but has no specific analysis.
 - “Floating Gate vs Charge Trap” is widely reported by Micron
- Sandisk reported BICS process for many years. It is unclear of process specifics for units currently being sampled (other than 48L)
- **RECOMMENDATION: Ignore the hype!**
 - Density and Die Size are the key cost metrics and both are available after sampling. Wait for real revenue shipments announced at earnings report

Cost summary

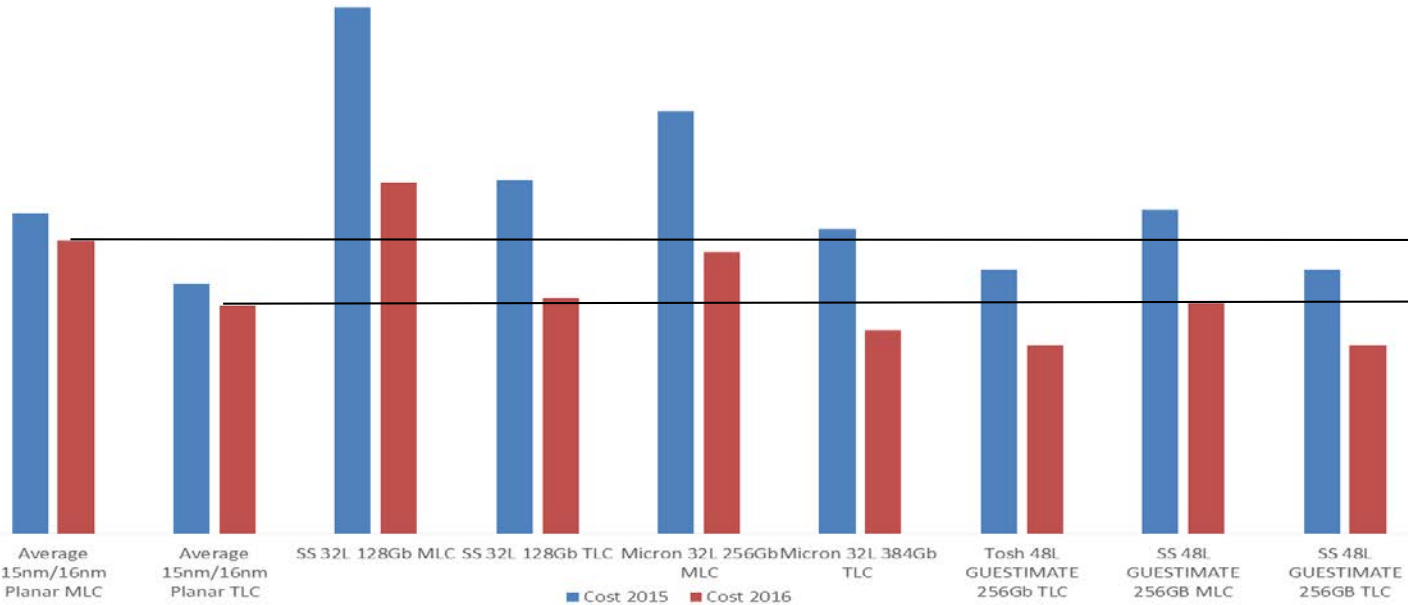
- Planar yields give them a cost advantage. Yields are modeled to be significantly higher for planar in 2015.
 - Planar costs are lower than 3D in 2015 and early 2016.
 - Planar TLC extends this advantage
 - Toshiba small 15nm die size is an advantage
 - Micron mature 16nm process is an advantage
- 32L TLC must be competitive with planar MLC.
 - Target is that TLC quality on 3D NAND is equivalent to MLC on 2D. This is key to 3D cost effectiveness
- 48L+TLC+HVM yields gives 3D large cost advantage
 - Starting in Mid 2016. For high densities (256Gbit+)



August 2015 Cost Summary (\$/GB)

Announces or Reported Technologies

NAND Cost Comparison



3D NAND costs higher in 2015

10-20% lower in 2016

TLC+48L Required

2016 Planar MLC

2016 Planar TLC



Impact of Cost on 3D Ramp

- 3D NAND will be <<5% for all companies but Samsung in 2015
 - This will be confirmed in earnings announcements
- Due to high density, 3D NAND will not be dominant in 2016 or 2017
 - ~20% of NAND goes to SSDs, which is primary 3D target
- 3D Industry conversion prediction
 - <18% of Industry Bits in 2015*
 - <25% of Industry Bits in 2016
 - <50% of Industry Bits until at least 2018.
- 3D NAND allows cost NAND reduction to continue.
 - There will be not be a cost tipping point
 - TLC, 15/16nm ramp is dominant cost reduction mechanism until then

- 3D NAND allows significant future cost reduction
- Costs for Planar are lower than 3D Today and into 2016
- TLC is required to extract benefit of 3D NAND
- 48L+TLC+Mature yields makes 3D NAND the cost leader in late 2016