Designing a Configurable NVM Express Controller/Subsystem

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“The IP enabled solutions provider”
The Mobiveil Team

• **Leadership**
  – Management with 25+ years experience in Semiconductor/Silicon IP/Systems/software
  – 100+ member development team with previous experience in high speed interfaces located in US & India
  – Previously founded GDA Technologies, Inc and grew to strong IP and Services group, 500+ engineers strong.

**Key differentiators**

Developed several highly configurable key high speed IP blocks in the last 10+ years (PCI Express, Hyper Transport, Serial RapidIO, SPI4.2, DDR4/3, Flash Controllers etc)

**Locations**

**Headquarters in Milpitas, CA**
India design centers: Chennai & Bangalore
Sales: Offices/Reps worldwide
NVMe SSDC Subsystem
Mobiveil NVMe SSDC Subsystem

- On Chip AXI Interconnect
- On Chip APB Interconnect
- Inter block AXI Interconnect

Company Overview
NVMe SSDC Subsystem
NVMe Features & Configurability
IFC
Summary

UNH Certified

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Mobiveil Subsystem IP Advantages

**Superior Technical Solution:** Most Feature rich IP, Complete Customization and delivery Solution

**Market leading & most exhaustively proven cores in the market:** Industry leaders are using these cores

**Consortium Participation:** NVM Express- Member, RIO – Member, PCISIG – Member, HMC - Member

**Support:** Clear IP Focus & Worldwide Support

**3rd Party Partnerships for complete Solution:** (VIP PHY IP,s, FPGA, eASIC and SOC Partners)

**Standard Body Certified Cores:** All Mobiveil IPs are validated and certified: PCI Plug fest, UNH, RTA
NVMe - Features

- A Register level interface that allows host software to communicate with a non-volatile memory subsystem
- Defines a standard command set for use with the NVM subsystem
- Optimized for Enterprise and Client solid state drives, typically attached to the PCI Express interface
- Defines Pair of Submission and Completion IO Queues
- Defines parallel operation by supporting up to 64K I/O Queues with up to 64K commands per I/O Queue.
- Defines many Enterprise capabilities like end-to-end data protection, enhanced error reporting, and virtualization
- Supports differentiated services, i.e., different qualities of service (QoS)Targets
- Supports Multi-Path IO and Namespace Sharing capabilities
- Supports Reservations
- Supports multiple name spaces
NVMe Configurability

- LBA & Meta Data Size
- Number of IO Queues & Depth
- Vendor Defined Commands
- INTR/MSI/MSI-X
- Vendor Specific Command Arbitration
- Number of Flash Channels
- Reservations Support
- Multi-Path IO Support

Configurable IP Components

- Number of Flash Channels
- Reservations Support
- Multi-Path IO Support
- INTR/MSI/MSI-X
- Vendor Specific Command Arbitration

Vendor Defined Commands

Company Overview

NVMe SSDC Subsystem

Summary
NVMe Configurability

- HW/SW Partitioning
- Clock Frequency
- Re-Use of modular Components
- Interfacing with 3rd Party IPs
- Interfacing with 3rd Party VIPs
- Number of DMA Engines
- Data Path Width Support
- Efficient Buffering
Configurable NVMe Controller

- Address all Features
- Design, Implementation, Verification Effort
- Area, Frequency
- Latency, Bandwidth, QOS
Configurable IP Components
NVM Express Controller (UNEX)

Industry’s First IP to Pass UNH–IOL Certification
NVM Express (UNEX) Controller

- Highly Configurable
- Technology Independent

UNH Certified

Company Overview
NVMe SSDC Subsystem
NVMe Features & Configurability
UNEX
Summary
UNEX Features

- Compliant to NVM Express 1.1 specification
- Supports configurable number of IO Queues
- Supports configurable Queue depth
- Supports Round Robin or Weighted Round Robin with Urgent Priority arbitration mechanism
- Host memory page size support of 128MB
- Efficient and Streamlined Command handling
- Supports Fused Operations
- Supports All Optional Admin Commands
- Supports All Optional NVM Commands
- Supports Multi-Path IO and Namespace Sharing capabilities
- Supports Reservations
- Supports multiple name spaces
- Optional AXI interfaces for NVMe implementation in SoC
- Well defined Command Interface for local CPU to perform subsystem initialization and to handle all non-hardware accelerated commands
- Targets FPGA, Structured ASIC and Standard Cell technologies
PCI Express Controller (GPEX)
PCI Express (GPEX)

**Agenda**
- Highly Configurable
- Technology Independent
- System Validated

**Company Overview**

**NVMe SSDC Subsystem**

**NVMe Features & Configurability**

**GPEX**

**Summary**

- Gen1, Gen2 & Gen3 Endpoint
- Root Complex
- Dual mode
- Switch port
- Switch
- OCB Solution
- x1 to x32
- 180nm to 28nm
PCle-AMBA Bridge

- Highly Configurable
- Technology Independent
- System Validated
Transparent PCIe Switch

- Highly Configurable
- Technology Independent
- System Validated
DDR3/4 Memory Controller
DDDR3/4 Memory Controller

- Highly Configurable
- Technology Independent

Company Overview

NVMe SSDC Subsystem

NVMe Features & Configurability

DDR3/4 Controller

Summary

Configuration & Status Registers (CSR)

Multi Port Controller (MPC)

Base Controller (BC)

Port Arbitration (QoS)

WRITE DATA MUX

READ DATA DEMUX

WRITE DATA PATH

READ DATA PATH

Bank CTRL 0

Bank CTRL 1

Bank CTRL 2

Bank CTRL N

Configuration & Status Registers (CSR)

APB
DDR3/4 Controller Features

- Compliant with AMBA 3
- Compliant with DFI 2.1 Interface
- Supports QoS through various arbitration schemes
- Configurable and programmable address mapping
- Supports up to 4 ranks
- Supports following BC Clock to PHY Clock ratio
  - 1:1 (Full-rate Mode)
  - 1:2 (Half-rate Mode)
  - 1:4 (Quarter rate Mode)
- Supports Burst Length 4, 8, 16
- Supports Active/Precharge Power down
- Supports software and hardware driven Self Refresh entry and exit
- Supports Auto-refresh and per-bank refresh
- Supports ECC Checking and Correction (optional)
- Supports automated memory initialization
- Supports ZQ Calibration
- Targets FPGA, Structured ASIC and Standard Cell technologies
Integrated Flash Controller
Integrated Flash Controller

- Highly Configurable
- Technology Independent

Silicon Proven
Integrated Flash Controller
Features

• Flash Controller with eight chip selects
• AXI V1.0 Slave Interface
• Separate Bus Interface for register access
• Support for error and debug registers
• Supports NAND, NOR and GPCM (SRAM and ROM) devices
• Support memory banks of size 64KByte to 4 GBytes
• Write protection capability (only for NAND and NOR)
• Provision of Software Reset
• NAND Flash Features
  – x8/ x16 NAND Flash Interface
  – Support for ONFI-2.2 Asynchronous interface (8/16 Bit)/Source Synchronous interface (8 bit) and mandatory commands.
  – BCH code for 4 bit & 8 bit Error correction per sector of 512 bytes (Using GF-2^13 Galois field) and 24 & 40 bit ECC per sector of 1K bytes (Using GF- 2^14 Galois field)
  – Optional ECC generation and checking
  – Flexible timing control to allow interfacing with proprietary NAND devices
  – SLC and MLC Flash devices support with configurable page sizes of up to 8KB
PCIe NVMe SSDC Platform
Mobiveil NVMe SSDC Platform
Mobiveil NVMe SSDC Platform

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UNH Certified
Mobiveil at FMS 2014

- Bronze sponsor at FMS 2014- Booth # 721
- Announcement with Altera and Everspin on MRAM based solution
- Announcement with eASIC on making Mobiveil NVM Express IP available in their devices.
- To know more about Mobiveil NVM Express IP and SSDC Platform
  - You can visit Mobiveil booth (#721) for additional information
  - Visit Altera or Mobiveil booth for additional information on Everspin MRAM based solution
  - Speak to Silicon Motion booth to understand how they are accelerating their SOC design using Mobiveil NVM Express IP
  - Visit Mobiveil or Xilinx booth to know more about implementing UNEX in Xilinx platform
Thank you.

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