

Hardware NVMe implementation on cache and storage systems

Jerome Gaysse, IP-Maker



Agenda

- Hardware architecture
- NVMe for storage
- NVMe for cache/application accelerator
- NVMe for new NVM

Why NVMe for Data Center?

Intensive applications

Database

Virtualization

Big Data Analytics

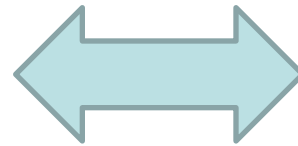
Data Center requirements

More performances (latency, IOPS)

Higher memory capacity

Non-volatile capabilities

Lower power consumption



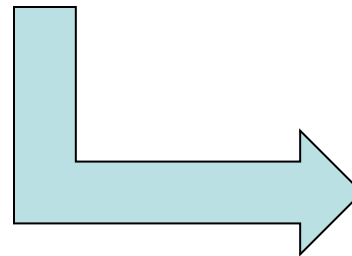
Emerging technologies

NandFlash

New memories (MRAM/RRAM)

New interfaces (NVMe)

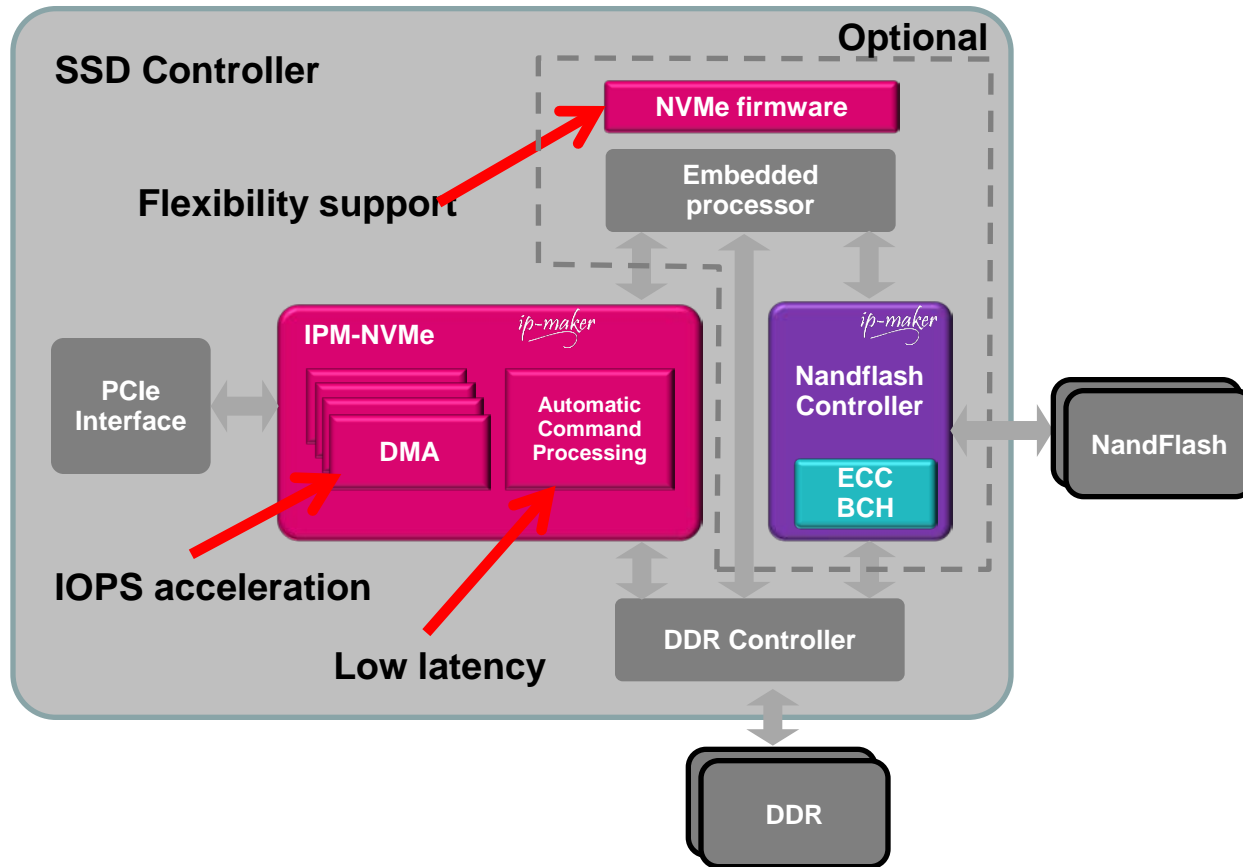
IP-Maker makes the bridge



PCIe SSD for

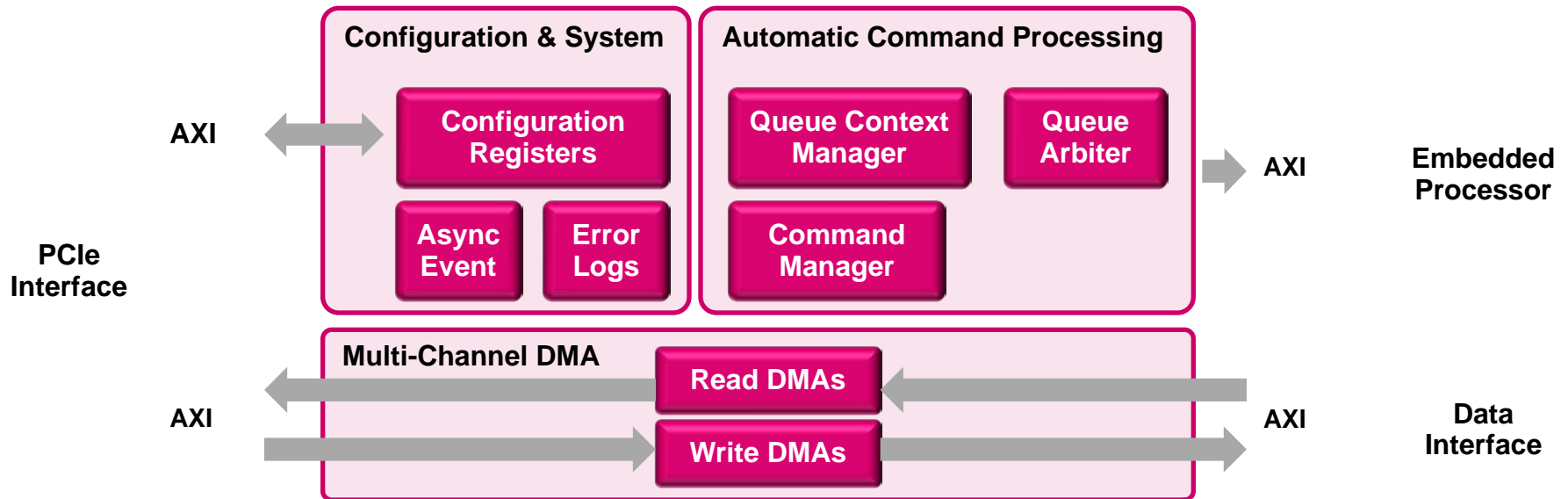
- **Storage**
- **Application acceleration**

NVMe SSD controller architecture



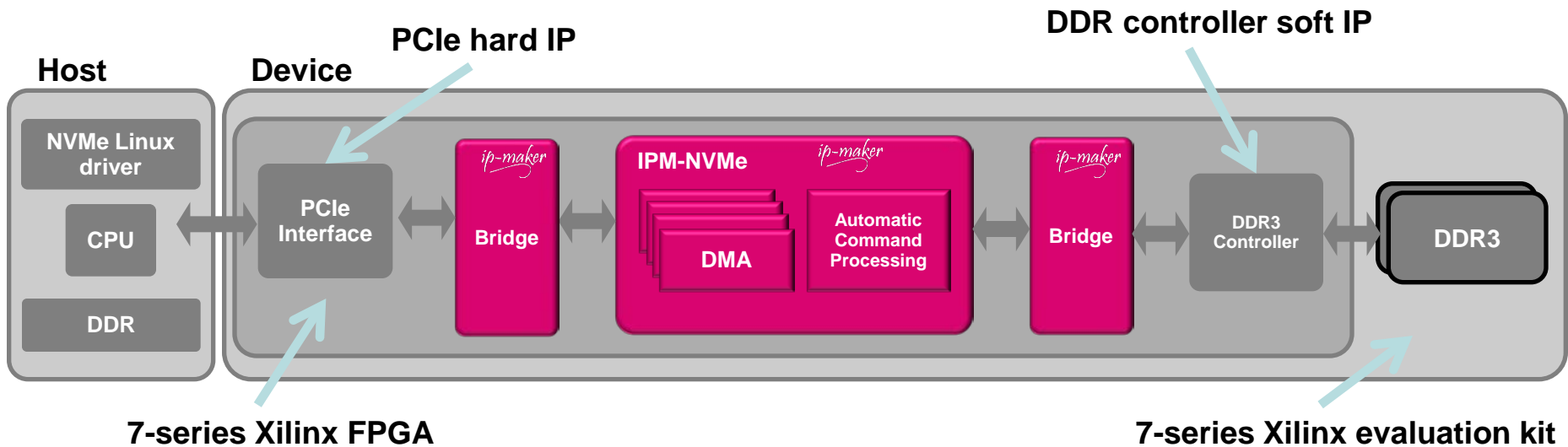
Hardware NVMe IP architecture

- Low latency with the automatic command processing
- IOPS acceleration with the multi-channel DMA



FPGA-Based reference design

- Gen2 x4 configuration performances:
 - IOPS: 350k
 - Latency: 12 μ s



How many kIOPS for a Gen2 x4?

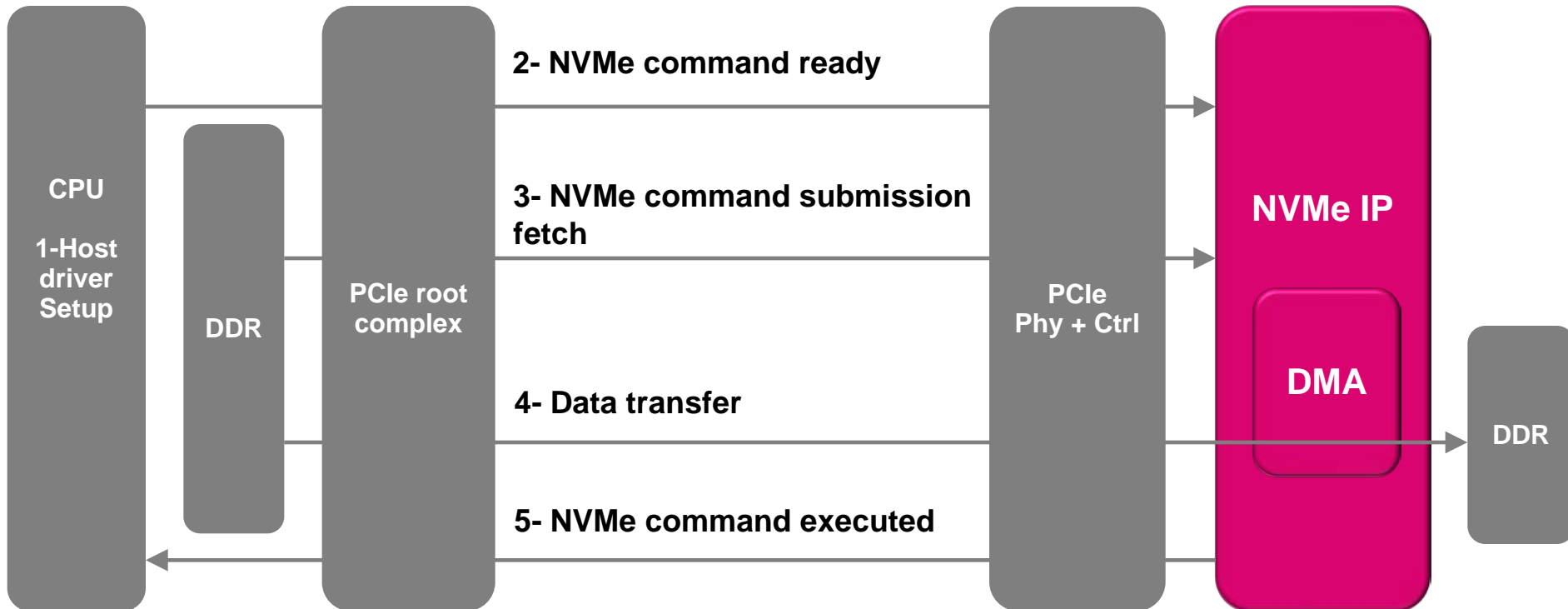
- Lane speed is 5 Gb/s => 20 Gb/s
=> **610kIOPS** max?

But,

- 8/10bit coding
=> **499kIOPS** max of data
- PCIe overhead (CRC...): 24B for a 256B payload
=> **446kIOPS** max of useful data
- 90% bus use
=> **400kIOPS** max
- And other...

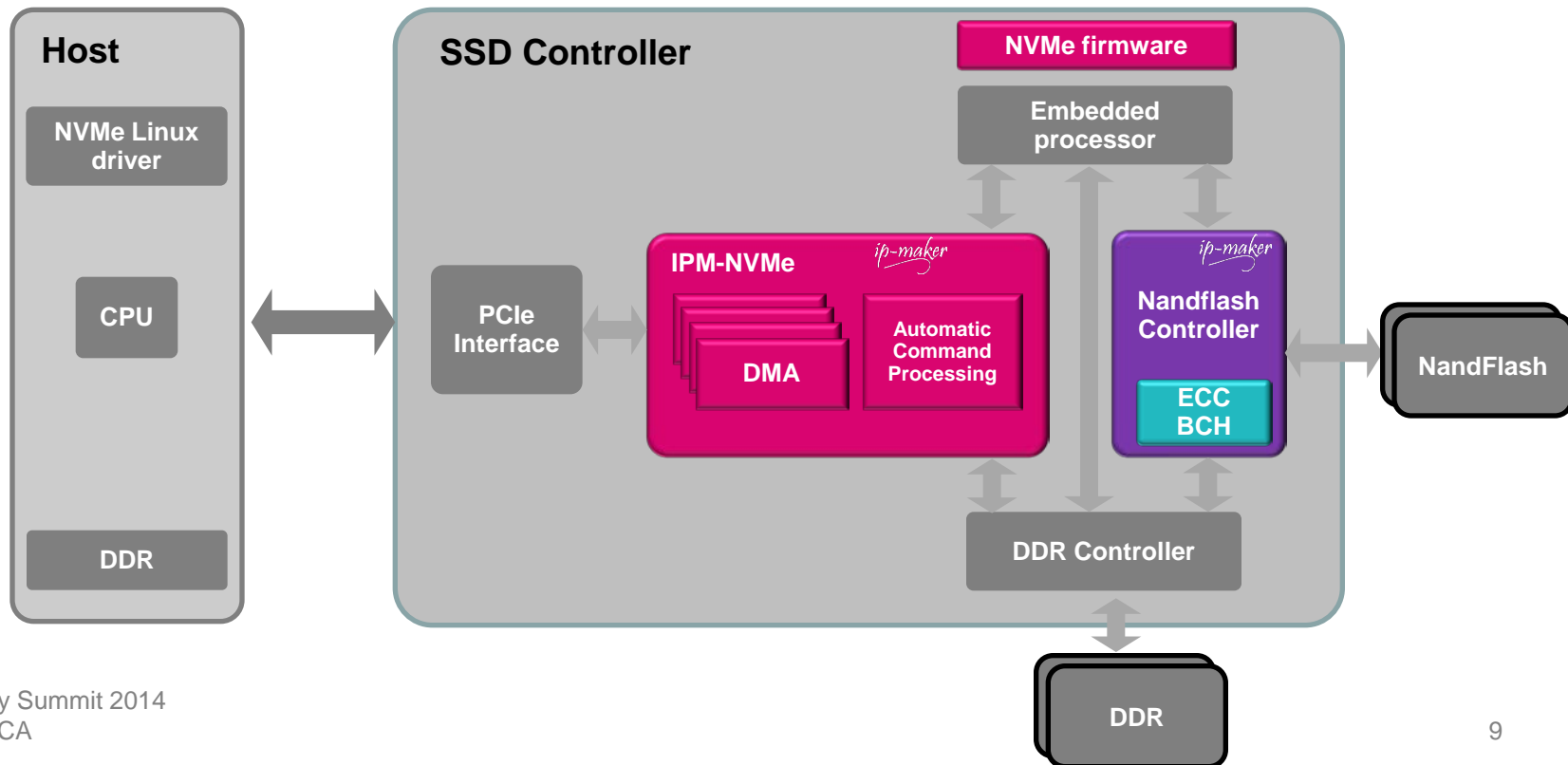
What is the latency for a Gen2 x4?

- 4 μ s for the host driver
- 8 μ s for all PCIe transactions
- Less than 0.1 μ s for the NVMe command processing



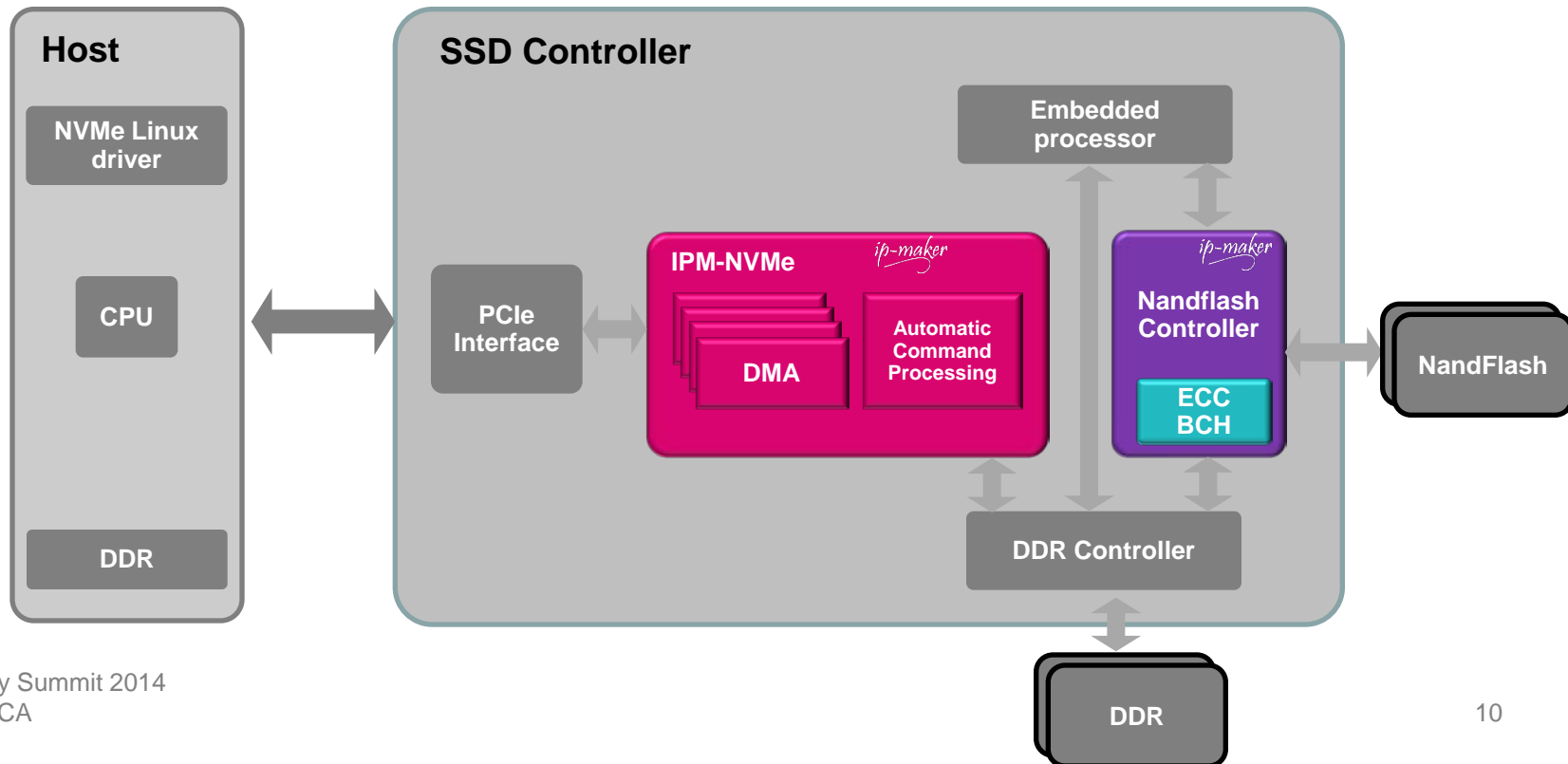
NVMe for storage

- Hardware NVMe for high performance
- Firmware NVMe for command flexibility



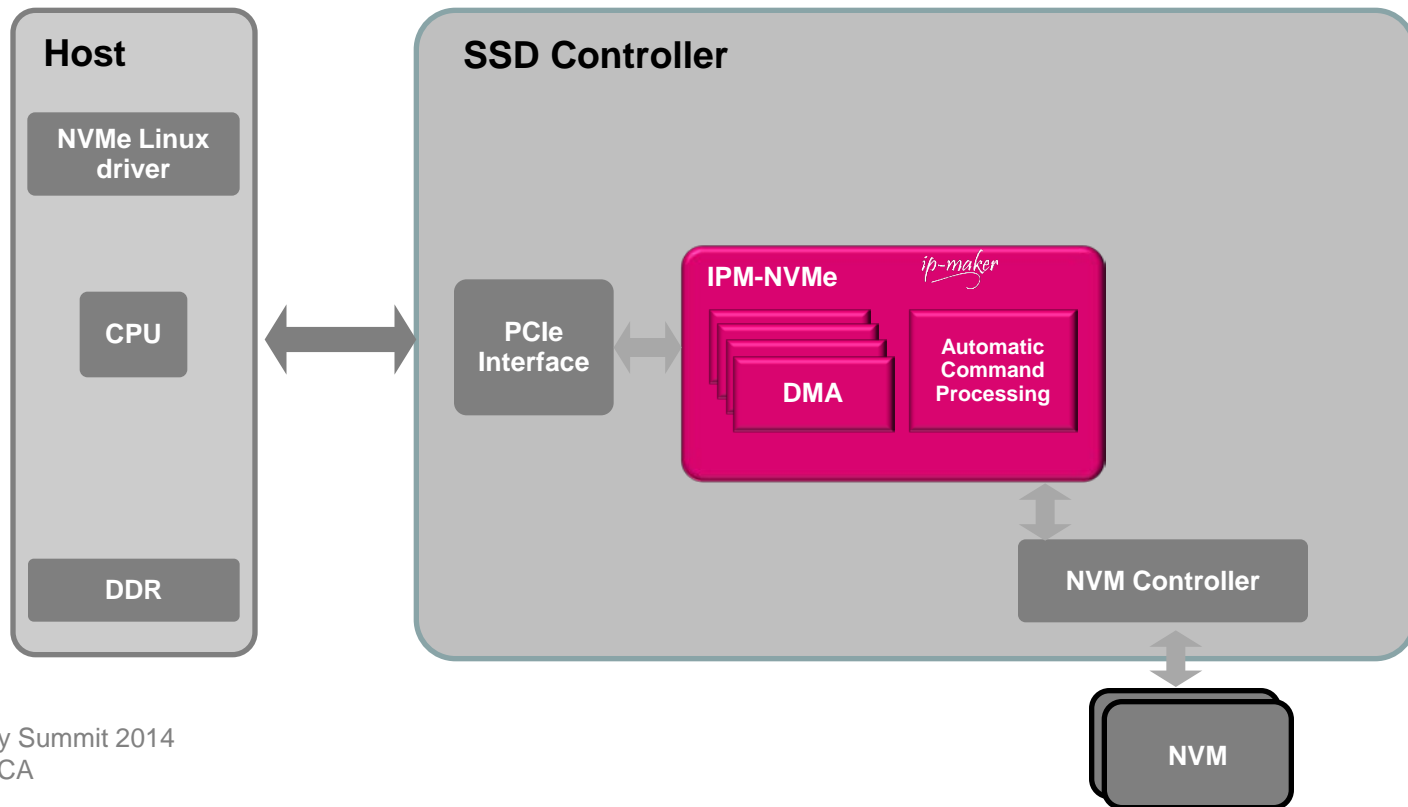
NVMe for application acceleration

- Hardware NVMe for high performance
- No need of flexibility: just performance
- CPU for NandFlash management



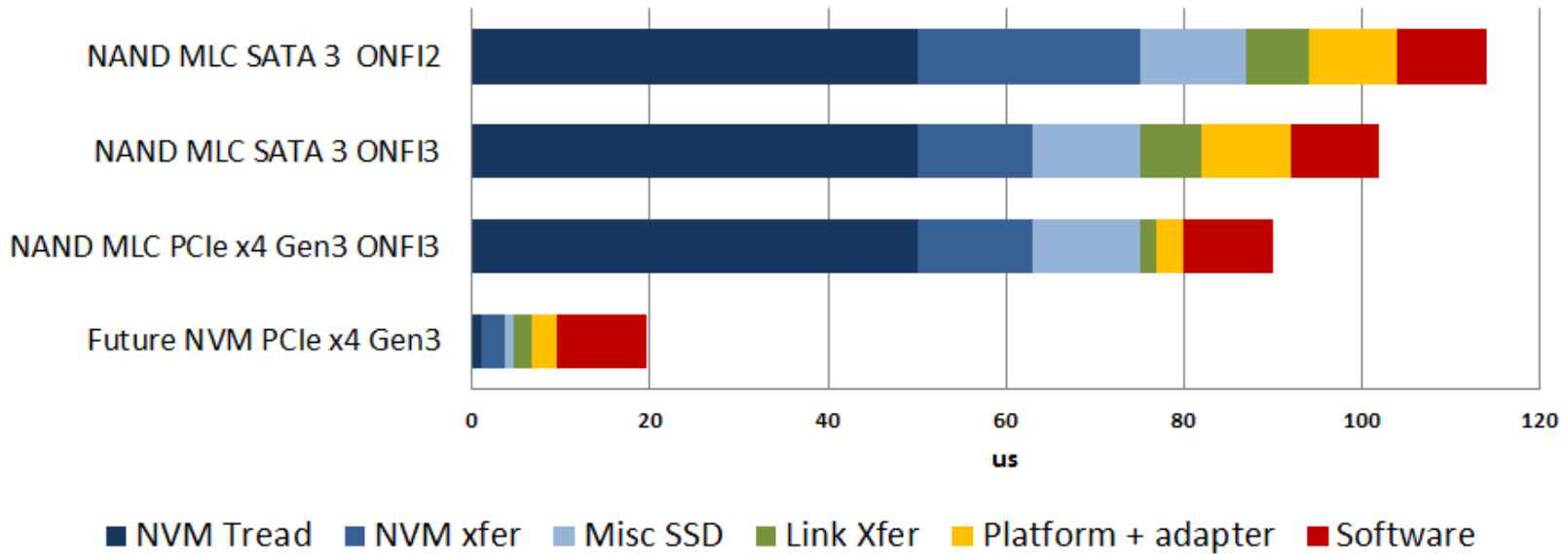
NVMe for new NVM (MRAM, RRAM)

- Simplified architecture
- Lower latency



Latency with different memories

App to SSD IO Read Latency (QD=1, 4KB)



Flash Memory Summit 2013, Amber Hufflan, Intel

- Benefits of a hardware NVMe architecture:
 - Ultra low latency with hardware acceleration for NVMe command processing
 - High IOPS with integrated multi-channel DMAs
 - High memory capacity with scalable design
 - New NVM capabilities
 - Low power consumption thanks to hardware acceleration



Thanks!

Visit IP-Maker booth #619
NVMe live demo!

Jerome Gaysse
Business Development Manager
jerome.gaysse@ip-maker.com
www.ip-maker.com