Reliable Flash Management and Error Correction

Evaluating different ECCs

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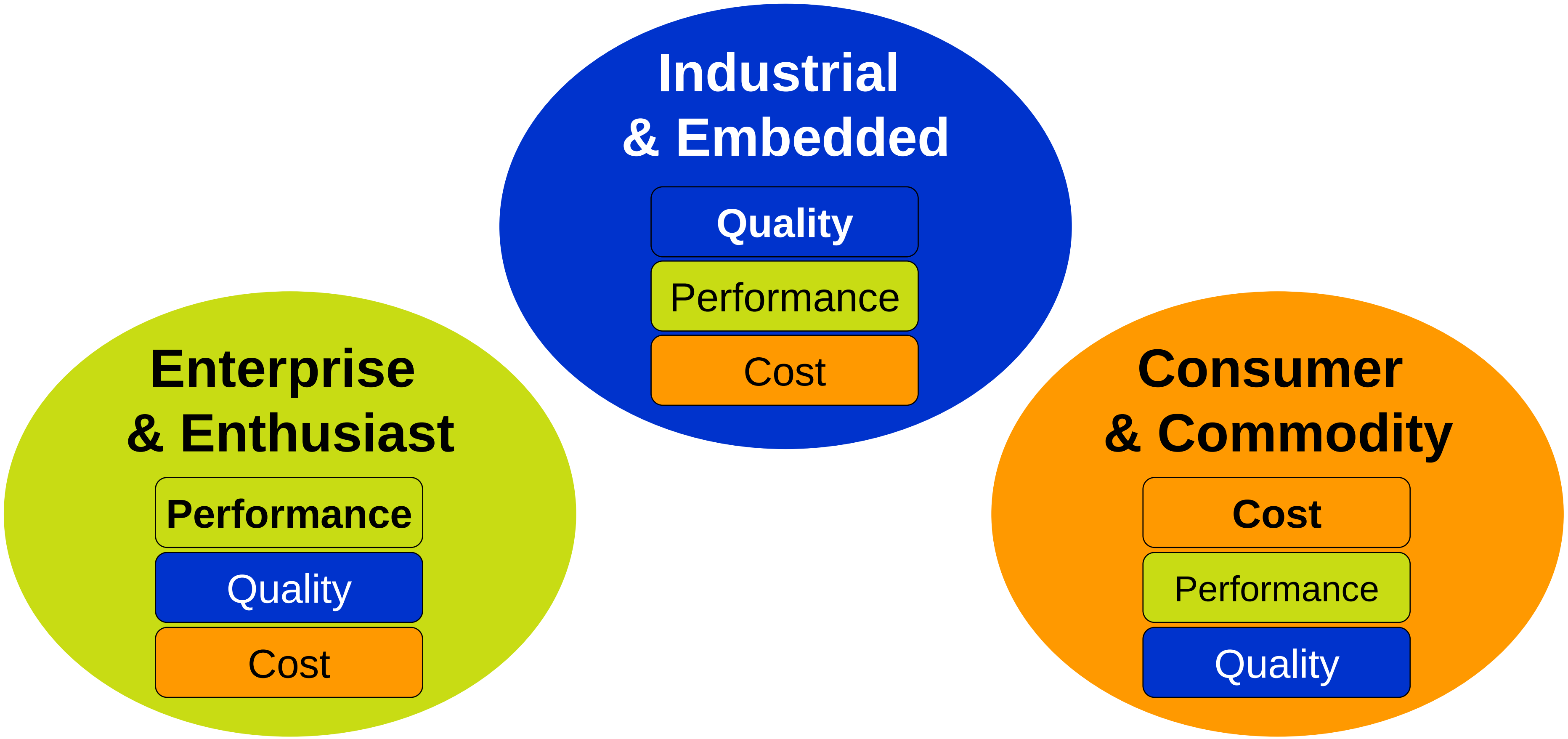
Hyperstone Focus

hyReliability™ - reliability first



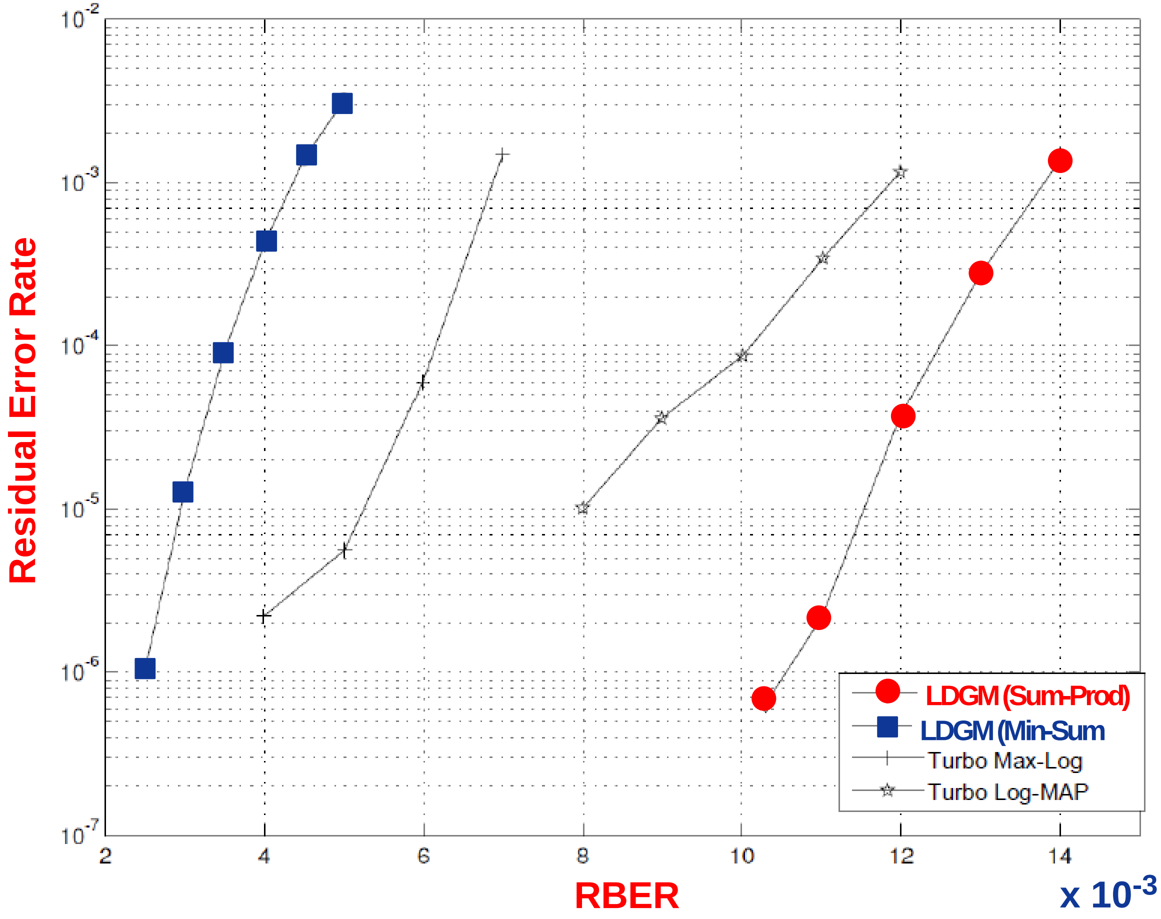
Evaluating ECCs

- UBER is not an adequate quality measure - BLER is
- Because of the error floor, LDPC codes require an additional outer code
- For the inner code performance we used the term Residual Error Rate
- Low-density generator matrix (LDGM) code used for comparison (lower encoding complexity, better correction quality with outer code)

Evaluating ECCs

- LDPC codes require knowledge of the actual RBER

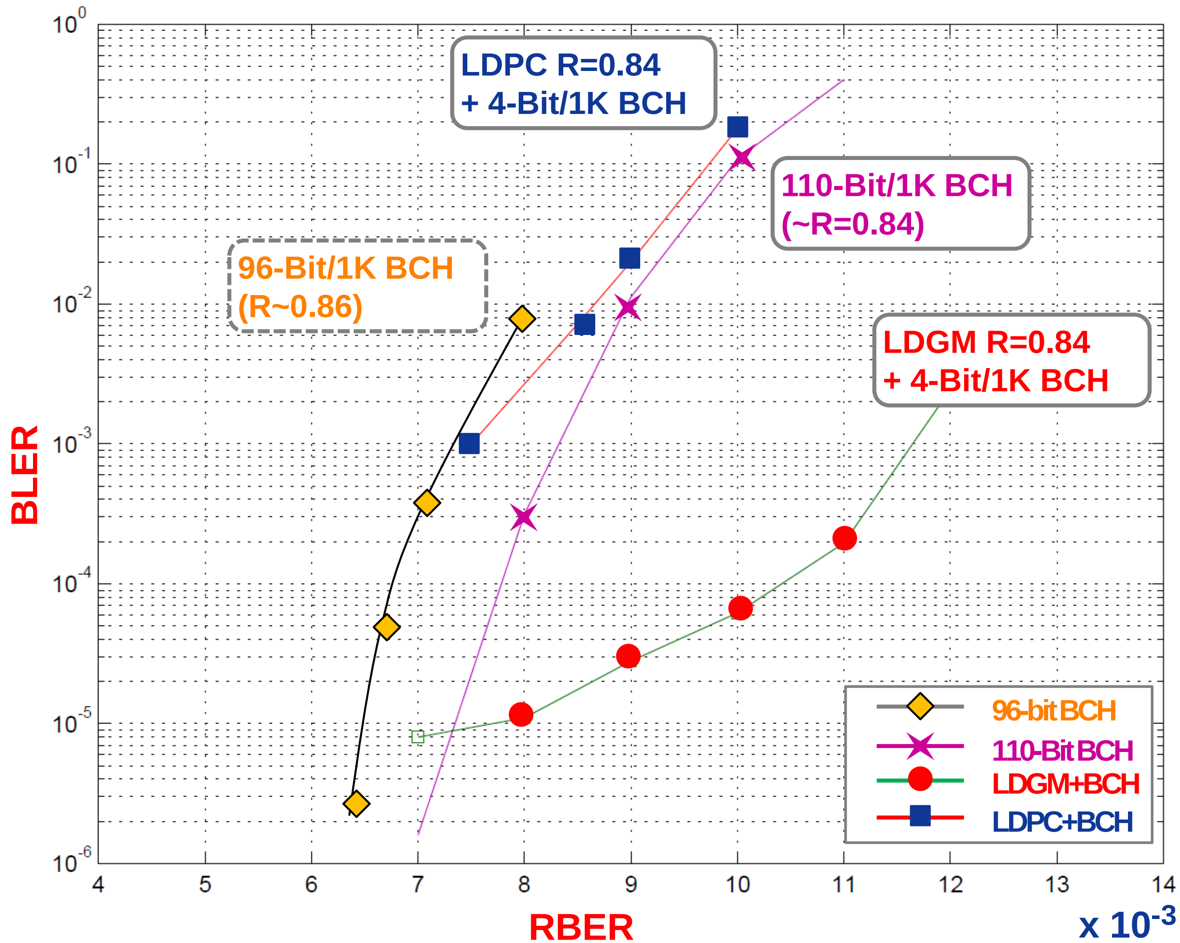
  - Min-Sum decoding correction quality relatively poor
  - Sum-Product decoding assumes perfect knowledge of RBER
  - This may be unrealistic over the lifetime of NAND



Evaluating ECCs

- LDGM/LDPC with an outer code compared to BCH

  - LDPC requires simulation, BCH can be calculated
  - For very high RBER, LDGM/LDPC could be superior
  - But how flexible or adaptable could this be in practice?



Evaluating ECCs

- Main finding: LDPC code's burstiness

Number of errors per block after decoding of the inner LDGM code

RBER	0	1	2	3	4	5	6	7	8	9	10	12	14	42	46	62	68	118
0.010	498404	1497	65	3	1	1	3	3	16	1	0	1	0	1	1	1	1	1
0.008	4993813	5965	167	2	1	2	11	13	24	0	1	0	1	0	0	0	0	0
Binomial	4993603	6393	4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

i.e. Block Error threshold for an outer 4-Bit BCH

Theoretical model (Binomial distribution, p=0.008): No residual errors beyond 2-Bit

BLER:
(For RBER 8 x 10^{-3} LDGM+4-Bit BCH)

~ 1×10^{-5}

Evaluating ECCs

- Conclusion: Reliably calculating a BLER and quantifying correction quality requires BCH codes
- LDPC error floor leads to residual errors after outer BCH decoding
- Under the conditions we investigated, LDPC codes outperformed BCH codes only under ideal conditions and only for very high RBER (>1%)
- For LDPC based ECCs it is difficult to prove a BLER of better than 10^{-11} because of simulation complexity

Conclusion

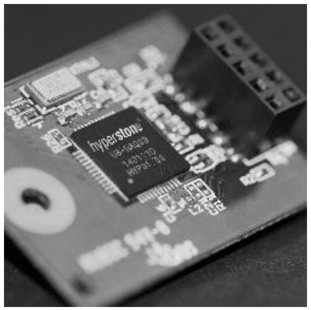
- BCH better suited considering:
  - Multi-generation and multi-technology Flash support
  - Widely varying environmental and temperature conditions
  - Correction quality and zero tolerance to delivering wrong results
  - Considerable correction speed and read latency
  - Power consumption
  - Robustness at the end of a NAND Flash Life
- BCH allows calculating a BLER based on any given RBER
  - For a RBER of 4×10^{-3} our 96-Bit/1K BCH achieves a BLER = 10^{-16}
- BCH complexity and gate count increases significantly with correction strength but it's a price worth paying

Related Reliability Features

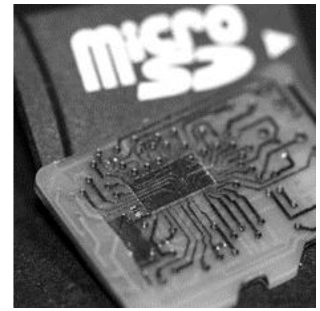
Background functions need low-power & fast ECC

- Near-Miss ECC
- Dynamic Data Refresh
- SMART Data output

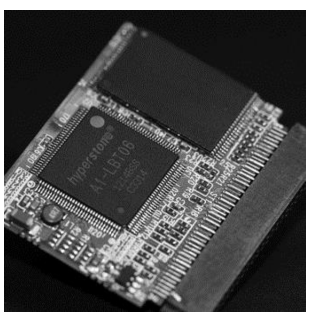
Hyperstone Products



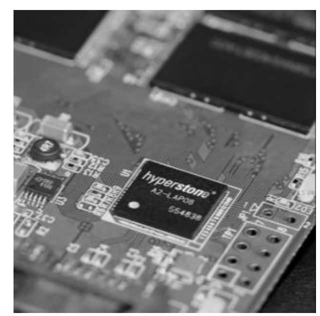
U8 – USB



S8 – SD/eMMC



A1 – CF/PATA



A2 – SATA

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Thank You!

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