Flash Quality Management in Enterprise Storage Applications

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Outline

- Enterprise Storage – Flash Technology & Quality
- Quality Management Overview
- 2D Floating Gate Quality & Reliability
- 3D NAND Quality & Reliability
- Flash Component Qualification Focus Items
- Flash Stacked Package Technology & Quality
- Summary
Enterprise Storage - Flash Technology Requirements

Quality & Reliability
Ensure Flash Memory with increasing density per generation meet Enterprise Server customer expectations End to End

Memory Density
System performance scales with Flash Memory Capacity, And Latency

Power/Thermal
System cooling constraints w/ High capacity Flash memory

Cost & Time to Market
- Achieve lowest overall cost for memory product over time
- Rapid responsiveness/ time to Market

Flash Technology Enablement
NAND Flash Quality Management – E2E Flow

- Flash Design
- Fab
- Wafer Test
- Package & Assembly
- Package Test
- Manufacturing SPQL Quality
- Field Quality
- SSD/Flash System Enabler
- Flash Supplier
- Closed Loop Failure Analysis

Flash Memory Summit 2014
NAND (cMLC, eMLC, SLC) Endurance & ECC Trends

- Endurance & Data Retention cycles have been decreasing with process shrinks 20~15nm node
- ECC requirements increasing exponentially with process shrinks
Advanced Flash Manufacturing & Quality

- Leading edge 300mm NAND fab manufacturing – driven by productivity, efficient, yield and quality requirements, typical fab capacity/throughput >100 Wafers per month
- Fully automated Manufacturing Execution System (MES) – integrates various sub-data/control systems in ensuring robust quality system
- Focus on SPC/APC based process controls & small drift controls – ‘nano’ scale process window control requirements needed for robust quality
- FDC (Fault Detection Control) methodologies critical for sub 30nm NAND & DRAM manufacturing quality control
- Rigorous & thorough equivalency practices required – across multiple fab locations spread out in widely different geo’s
- DFM (Design for Manufacturing) critical in areas of lithography OPC, Design rules, layout and pattern density effects
• Nanometer scale process controls critical for sub 20nm Flash Manufacturing
• SPC, APC, FDC Fab controls critical for advanced Flash quality
Flash Wafer Test

Wafer Burn-in
- High Temp wafer level B/I
- Screens for Wordline, Bit-line early life fails

High Temperature Wafer Test
- Trimming, Hard Row/Column defects
- Margin fails, Repair

Low Temperature Wafer Test
- Cell distribution at low temperature
- Weak contacts
Flash Package Test

Time Dependent Burn-in
- Defect screen/Erase status check
- Cell distribution at high temperature
- Peripheral and data path stress

Low Temperature Test
- AC/DC characteristics
- Functionality test

Diagram:
```
Time Dependent Burn-in
  ↓
Low Temp Test
  ↓
QA Gate
  ↓
Packing
```
NAND Floating Gate – Scaling Challenges

- As Floating Gate geometry shrinks, the same amount of charge loss causes larger Vt shifts – **causing endurance & data retention degradation with NAND scaling.**

- FG-FG capacitive coupling and interference.
  - 3D NAND Charge Trap Flash- workaround for this limitation

- Narrow FG-FG space doesn’t leave enough room for the two inter-poly dielectric layers.
  - Floating gate scaling challenge @ sub 15nm NAND

- Main challenge is cell endurance, data retention. Cell operation window and Program Disturb due to High program fields

- Commercial grade MLC @ 19-15nm targeted at ~3K endurance/1 Year data retention target spec – with Process Technology, strong ECC and Signal processing
Threshold Voltage and Flash Operations

- Vt distribution widened with technology node shrink
Floating Gate Charge Trap Generation & SILC

- Flash reliability governed by charge traps in Floating gate oxide
- At high cycle counts & low temperature, Stress Induced Leakage Current (SILC) dominates
NAND Reliability

- **Endurance** - Number of Program/Erase cycles a cell is expected to be able to withstand. Failure mechanism is caused by charge trapping in gate oxide. Commercial MLC NAND at 2X – 1X nm sustained @ 3K endurance

- **Data Retention** - Charge is lost on the floating gate over time. Block can be erased and reprogrammed. C-MLC spec’d @ 1 year, E-MLC @ 3 month with max pre-cycled condition

  **Affected mainly by three mechanisms.**
  * High temperature accelerates rate of charge loss.
    - Charge de-trapping can occur.
  * Stress Induced Leakage Current (SILC)
    - Degradation caused by P/E cycles
    - Voltage accelerated
  * Cell Disturb
    - Activity on adjacent pages or cells can cause gradual buildup of charge on floating gate

- **Program Disturb** – Charge collects on floating gate causing the cell to appear to be weakly programmed. Partial page programming accelerates disturbance

- **Read Disturb** – Pages not selected for read see elevated voltage stress. If enough charge collects on floating gate, cells can appear to be charged, causing a flipped bit

  **as geometry shrinks, the same amount of charge loss causes larger Vt shifts – challenge to endurance & data retention for sub 20 nm Floating Gate MLC NAND**

- **Early Life Fails** - i) Fab Particle driven SPQL Manufacturing quality focus  ii) Intrinsic Failure Modes
Flash Reliability Key Failure Modes - Vt distribution

P/E Cycle Charge Trap

High Temperature Retention (De-trapping)

Low Temperature Retention (SILC)

Early Life Defects
NAND Flash Comparison: 2D Floating Gate vs. 3D NAND

<table>
<thead>
<tr>
<th>Cons</th>
<th>Pros</th>
</tr>
</thead>
<tbody>
<tr>
<td>Erase Time</td>
<td>Program/Read Time</td>
</tr>
<tr>
<td>Data Retention</td>
<td>Vt Distribution</td>
</tr>
<tr>
<td>Architecture (block size)</td>
<td>Endurance</td>
</tr>
</tbody>
</table>

Forward Insights, “Cost and Investment Implications of 3D NAND”
Plug size and Tox should be tightly controlled to minimize 3D cell performance variations.
Flash Packaging Technology – Key Directions

- High reliance on stacked packaging – 4DP/8DP in production, development focused on 16DP package enablement

- 16DP stacked packaging – Enabling 2 Tera Bit Flash package (using 128Gb MLC Flash die @ 2y/1ynm node)
  - Thin Si manufacturing quality focus
  - Stress management – package design FMEA

- Flash TSV Stacked package – viewed as future package technology, benefit in power consumption & performance gain
Flash Qualification Overview

**Process Reliability**
- TDDB
- Electromigration
- Stress Migration
- Hot Carrier
- NBTI
- Vt Stability
- Maverick Lot Protection

**Die Qualification**
- Functional Test
- Precondition
- Cycling 25C
- Cycled Read Disturb
- Low-Temp Data Retention
- High-Temp Data Retention

**Package Qualification**
- Functional Test
- Precondition
- HAST
- High-Temp Storage
- Temp Cycle
- Bond Integrity
- MSL
- Solder Ball Integrity
- Solderability
- ESD
- Latchup

* JESD47 Flash Qualification Flow
Summary

- E2E Flash quality critical to enterprise storage applications.

- Pervasive shift left quality focus – Design, Fab process, Wafer Test, Package test critical for Flash Quality management at sub 20nm node

- Understanding 19-15nm 2D Floating gate reliability combined with Flash controller capabilities critical in enterprise storage technology enablement in 2014-2016 timeframe

- 3D NAND technology will allow Flash scaling to sub 15nm node – focus on 3D NAND failure modes and long term reliability capabilities critical for industry enterprise storage technology applications in 2016+ timeframe

- E2E Flash Quality management approach – including flash supplier quality, Manufacturing/SPQL, Early life and EOL reliability critical