New SSD Controller with eMMC array

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Today’s SSD Controller ➔
Driving Flash Array

We Pursue: Higher Density and Higher Speed
However, we are facing problems as following……
Problem (1)

- Higher Density and Higher Speed ➔ Driving More Flash chips ➔ Heavier Bus Load ➔ Limited Bus Speed

(Serious for DDR/Toggle interface)
- Higher Density and Higher Speed
  - Driving more flash buses in parallel
- More PADs/PINs
  - Limited Die Size,
  - Limited Package Size
  - Limited Package Cost
  - Limited PCB Space
- PAD or Core limited Design?

Flash Bus Pads: Data 8 wires, Control signal 7 wires, at least 2 pads for power and ground. Total: 17 PADs

PAD number for N channels: \(17 \times N\)
- If \(N = 8\), PAD number is 136
- If \(N = 16\), PAD number is 272
- If \(N = 32\), PAD number is 574, ……
Catching fast-changing flash datasheets

- Flash is continuously and frequently updated from 65nm ... 45nm ... 35nm ... 25nm ... 19nm ... 15nm ...
- All keep changing: endurance, ECC, wear-leveling, .......
- Controller vendor’s head-ache:
  - Expensive tape-out cost...
  - Long tape-out period ...
  - Exhausting workload...

Hiii, Crazy Guy, Could you have a rest?
Solution

SSD controller + eMMC Array
SageMicro’s SSD Controller ➔ Driving eMMC Array
## Advantages

<table>
<thead>
<tr>
<th>Compare items</th>
<th>SSD with Flash Array</th>
<th>SSD with eMMC Array</th>
<th>Advantage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Single package’s Max. Density</td>
<td>32GB</td>
<td>128GB</td>
<td>Higher Density</td>
</tr>
<tr>
<td>Single package’s PIN count</td>
<td>17</td>
<td>12</td>
<td>Less Pin Count</td>
</tr>
<tr>
<td>Flash Management Algorithm?</td>
<td>Mandatory</td>
<td>Optional</td>
<td>Less Flash management</td>
</tr>
<tr>
<td>New controller for new flash?</td>
<td>Possible</td>
<td>No</td>
<td>Controller not changed</td>
</tr>
<tr>
<td>New firmware For new flash?</td>
<td>Possible</td>
<td>No</td>
<td>Firmware not changed</td>
</tr>
</tbody>
</table>

Build 1T SSD?  
Just put 8 eMMC modules on board, each eMMC with 128GB density..
# SageMicro’s SSD Controller Family

<table>
<thead>
<tr>
<th>Part#</th>
<th>Interface</th>
<th>Flash or eMMC</th>
<th>Channel Number</th>
<th>Mass Product Date</th>
<th>Package</th>
</tr>
</thead>
<tbody>
<tr>
<td>S681</td>
<td>SATA-II</td>
<td>Flash</td>
<td>1,2,4,5,8,10</td>
<td>Oct. 2012</td>
<td>BGA207</td>
</tr>
<tr>
<td>S685</td>
<td>SATA-II</td>
<td>Flash</td>
<td>1,2,4,5</td>
<td>Dec. 2013</td>
<td>QFN88</td>
</tr>
<tr>
<td>S881</td>
<td>PCIE Gen-II</td>
<td>Flash</td>
<td>1,2,4,5</td>
<td>Nov. 2014</td>
<td>BGA256</td>
</tr>
<tr>
<td>S661</td>
<td>SATA-II</td>
<td>SD/eMMC</td>
<td>1,2,4,5,8,10</td>
<td>Oct. 2012</td>
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<td>BGA256</td>
</tr>
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</table>
Cost Effective?

- eMMC = eMMC controller + Flash.
- eMMC price > flash?
  Maybe, but not always…

Low quality?

- eMMC original for consumer application.
  But, JEDEC is making it for high-end application:
  - Speed ➔ DDR,
  - New Commands ➔ SSD like
  ……
Future Expectation:

JEDEC provide more eMMC features for SSD application like TRIM.

- eMMC is no longer “low quality” consumer concept.
- eMMC will be fine-tuned to embedded module for storage system.

Make your SSD modularization by eMMC.
Believe me, I am serious ➔
I am not joking ...

Cook Your own SSD by TF Cards.
Thank You!

Any questions?
Please feel to contact me by

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