

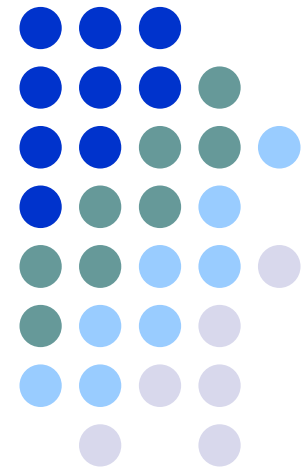
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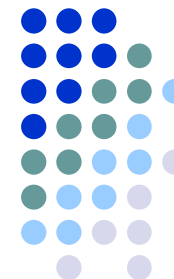
Flash Memory System Redesigned for Big Data

August 2014

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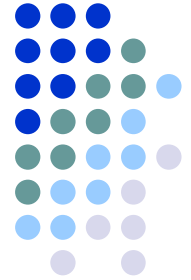
Axel Kloth, President & CEO SSRLabs





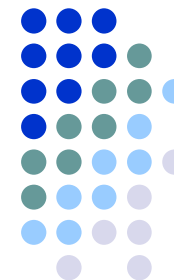
Overview

- Big Data is defined as
 - Large unstructured data with
 - High growth rate.



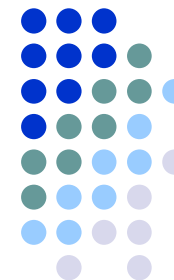
Big Data Implications

- Unstructured data equals random distribution of data across all addresses in the address space.
- Random accesses to random addresses decrease efficiency of caching strategies which rely on spatial and some degree temporal locality.



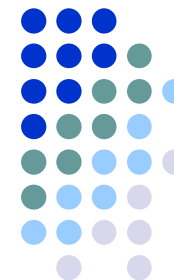
Technology Implications

- Large unstructured data in large memory arrays -> very low spatial locality -> low caching efficiency.
- Multiple multi-core processors or many-core processors working on a large unstructured data set in multiple large memory arrays -> even lower spatial locality in each level of cache, including shared cache.
- Since caching is not as efficient in those applications, high bandwidth and low average latency to the entire memory array are crucial.



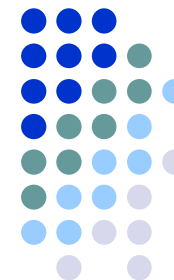
Theoretical Solutions

- Ideally, all data is held in registers. That requires new processors.
- The second-best solution would be all SRAM memory. This is prohibitive from a power and cost standpoint.
- The third-best solution would be a DRAM-lookalike solution.
- However, DRAM (particularly SSTL-2-attached) in the TB range still consumes too much power.

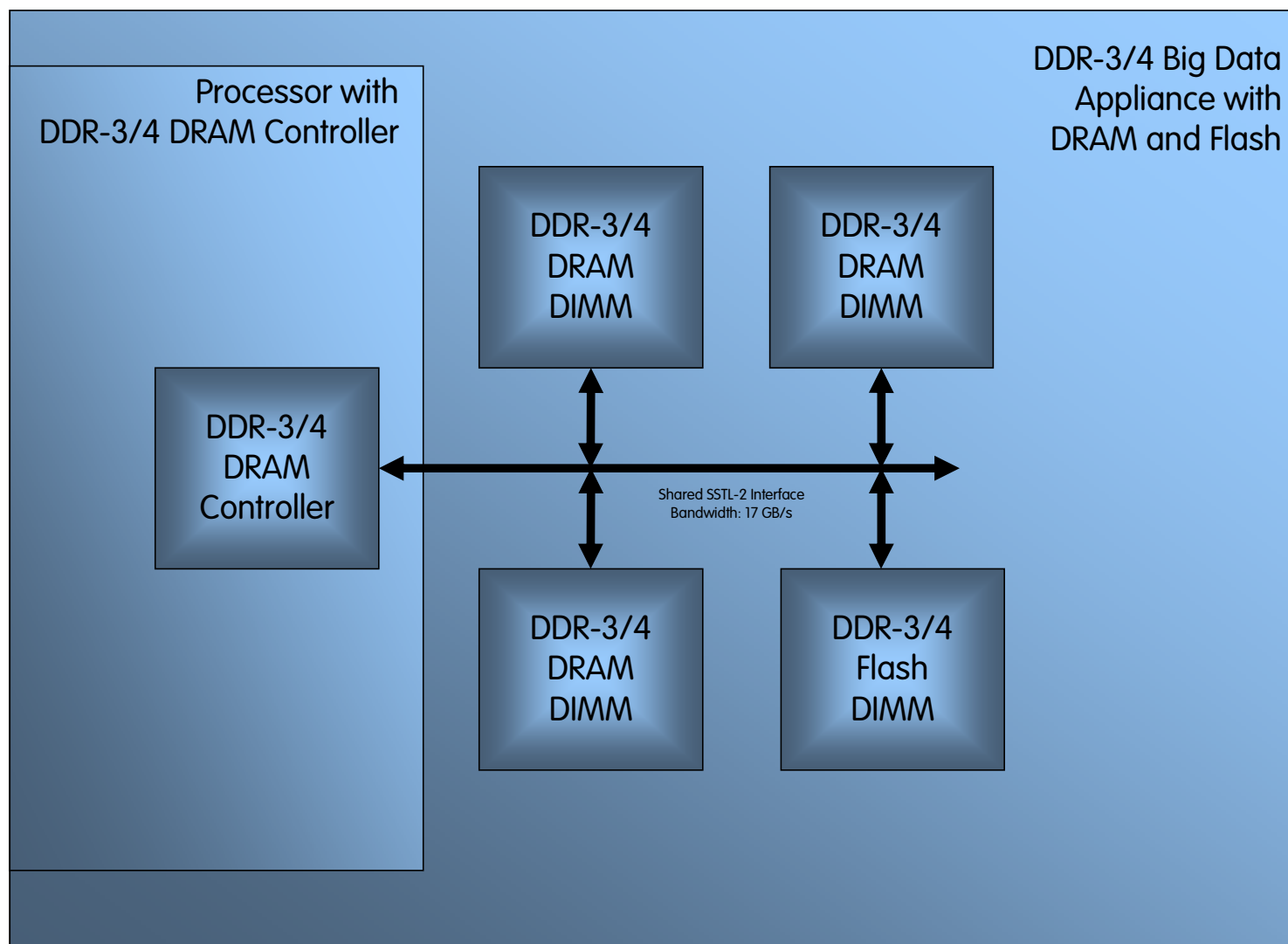


Practical Solutions

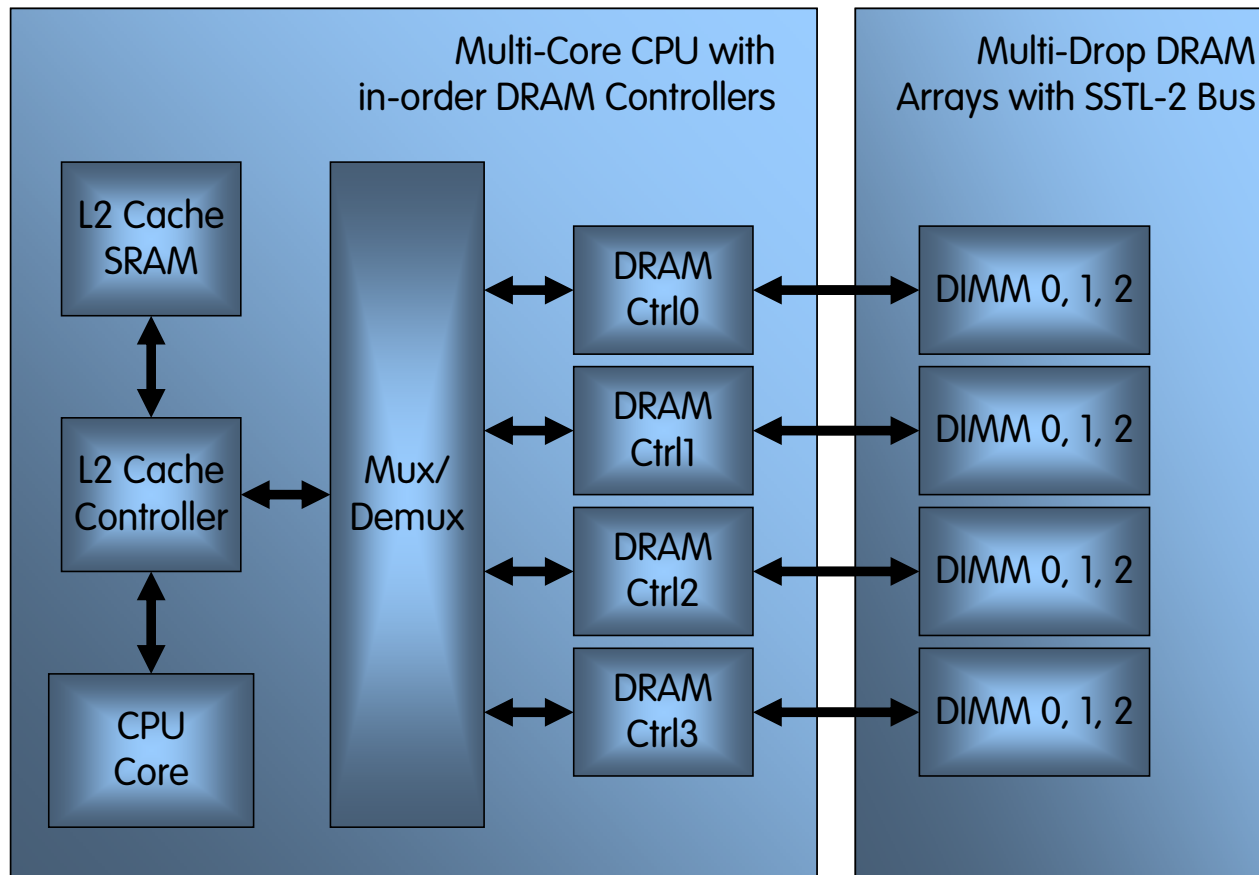
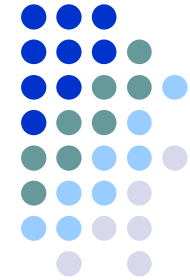
- DRAM-like memory arrays that consume less power at higher densities would solve the problem.
- Direct attachment to the CPU is preferred over SAS, SATA or PCIe for latency reasons.
- Even if a DRAM-like solution has a slightly higher latency than DRAM at a substantially higher density it can improve performance.
- Any mass storage access that is rendered unnecessary will improve performance.

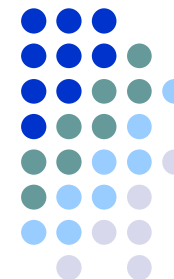


Current Processor and DRAM

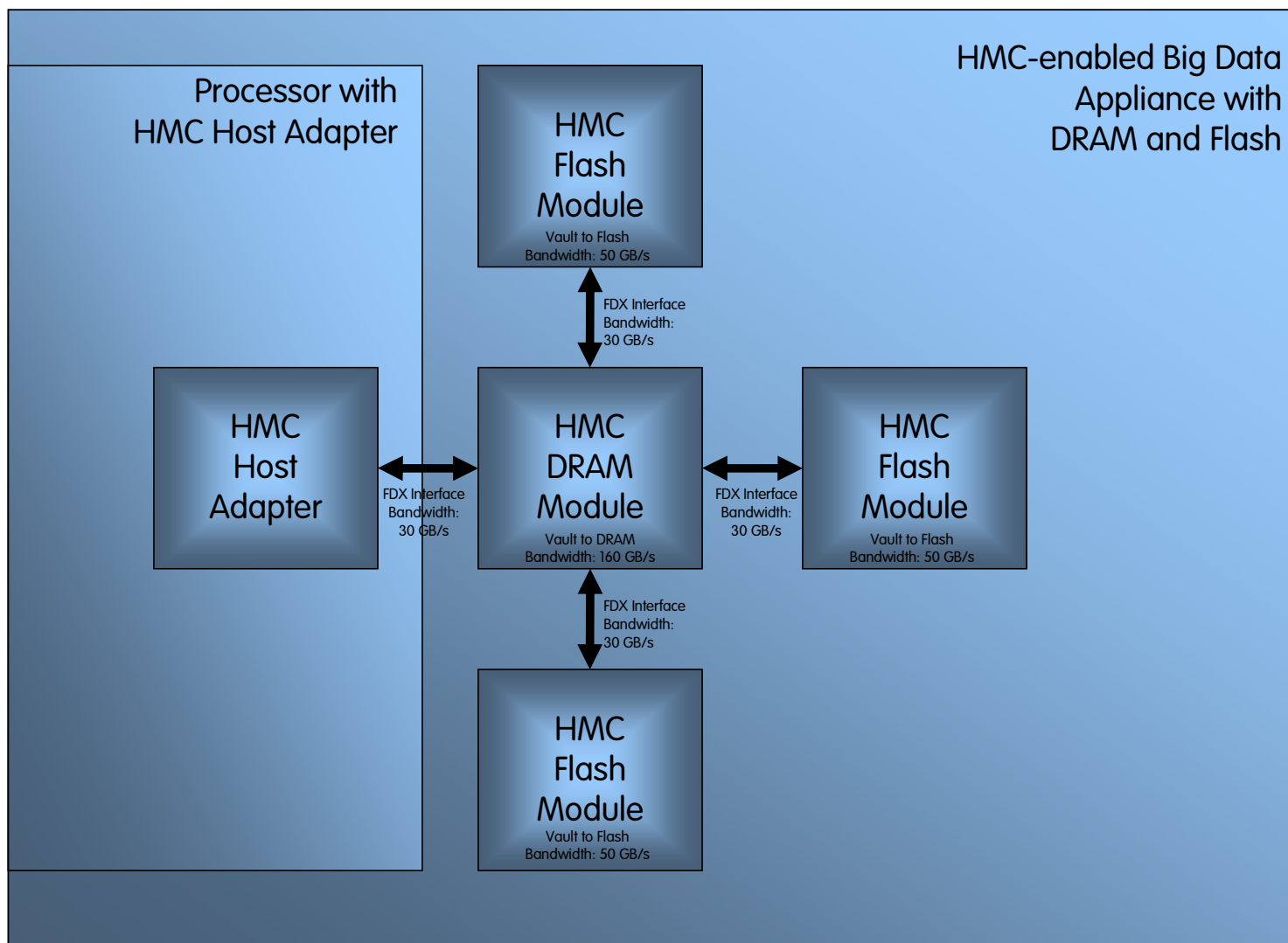


Current Processor and DRAM 2

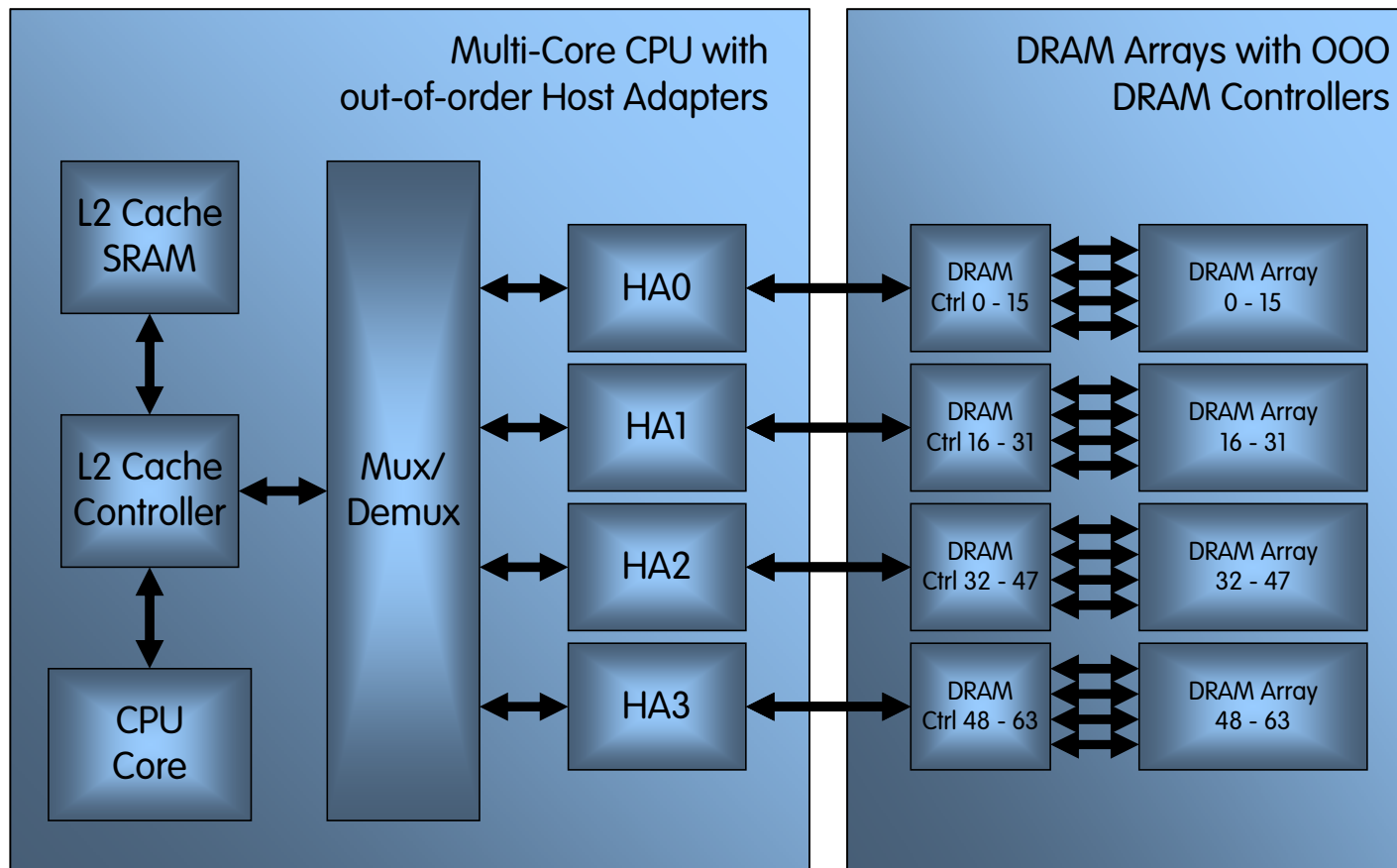
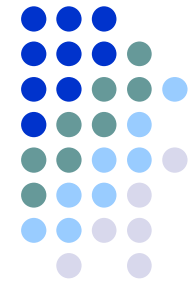


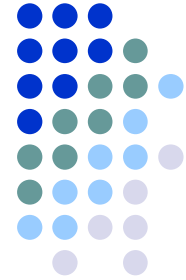


HMC Processor and Memory

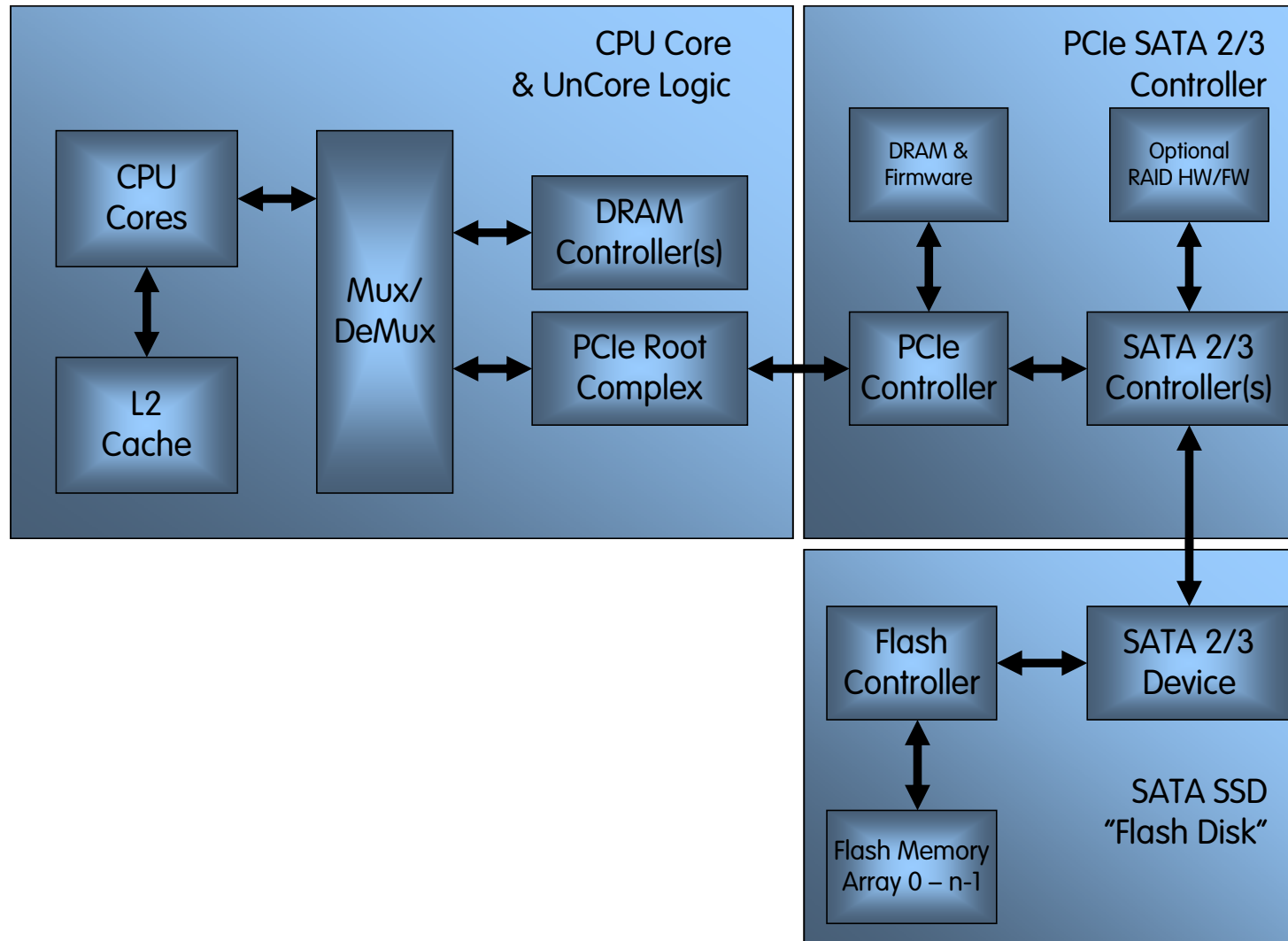


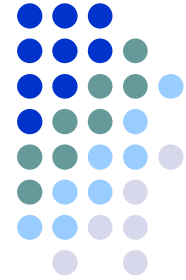
HMC Processor and Memory 2



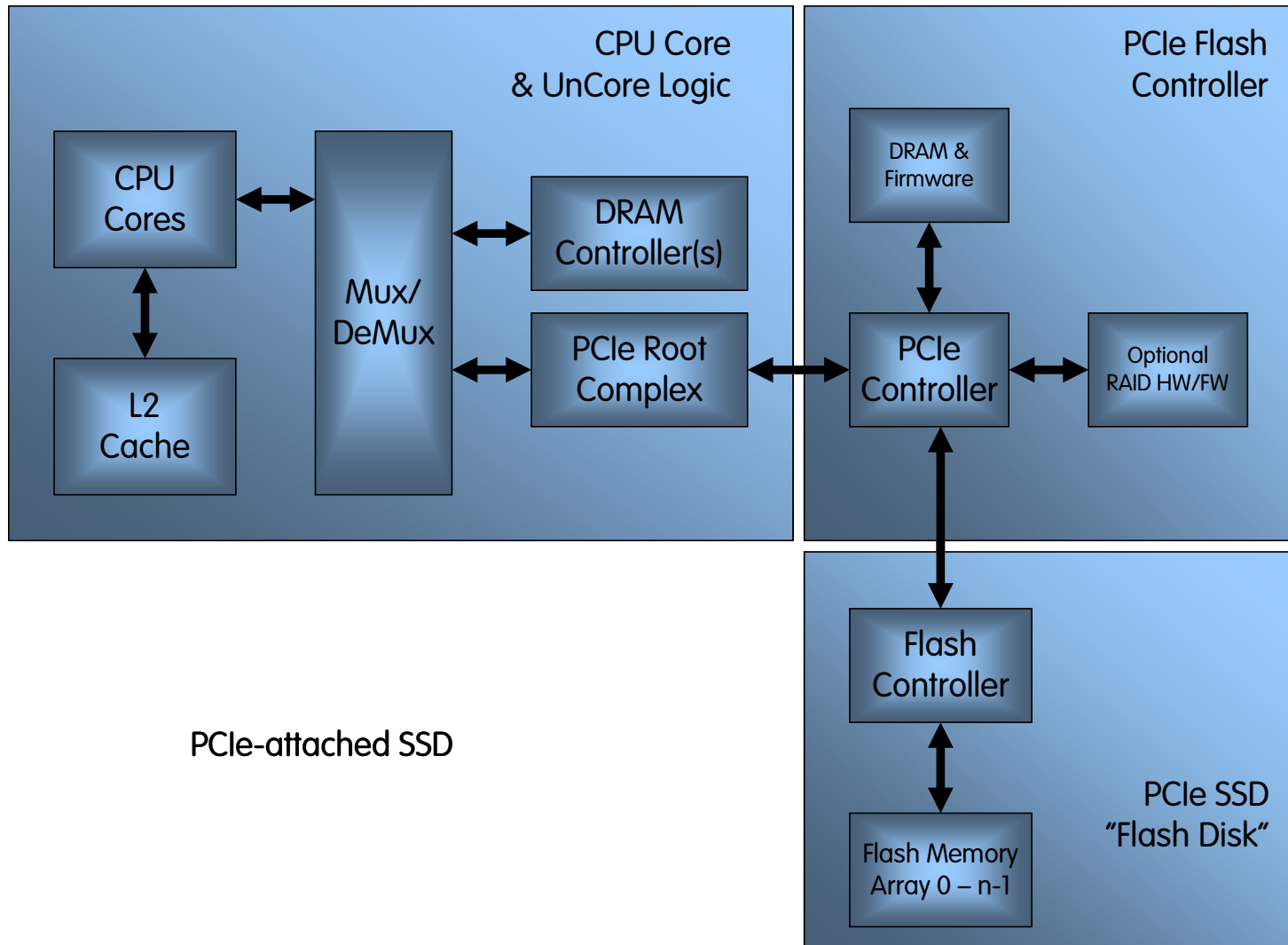


SATA-attached SSD

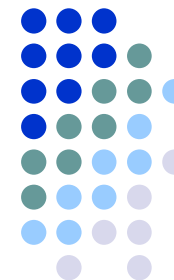




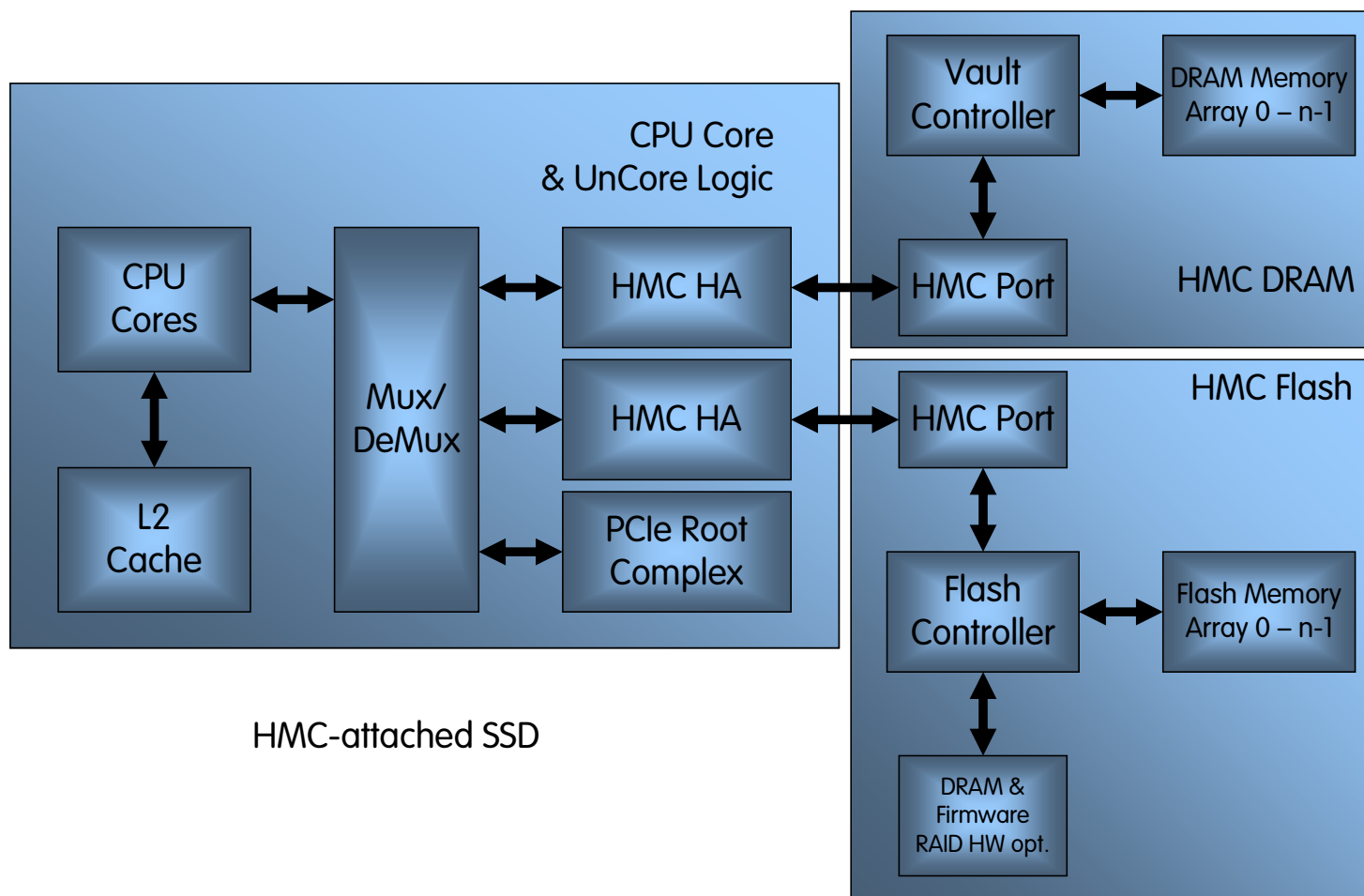
PCIe-attached SSD



PCIe-attached SSD

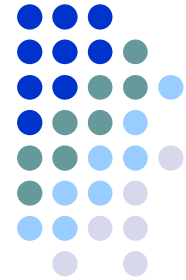


HMC-attached "SSD"



HMC-attached SSD

Legalese



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