Thermal Consistency Challenges in Testing High Wattage Enterprise SSDs

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Thermal Consistency for Endurance Test of SSDs

- Endurance test definitions require thermal consistency across SSDs during entire test
  - ±5 °C per JEDEC (JESD218A)
- PCIe SSD power spec is **up to 25W**
  - 4X to 5X more than some SATA SSDs
- Test setup with single DUT thermal control is ideal, but expensive
- Multi-DUT thermal chambers are more cost effective, but introduce thermal consistency challenges
  ➢ This presentation explores these challenges
Why Thermal Stress Test

• For endurance testing, thermal stress accelerates the time to fail (greatly shortening test time)
• Acceleration adheres to the Arrhenius equation

Arrhenius Equation
Predicting Temperature Dependence on Time to Fail

\[ t_f = A e^{E_A/kT} \]

- **\( t_f \)**: time to fail
- **\( A \)**: acceleration factor
- **\( E_A \)**: activation energy;
- **\( k \)**: Boltzmann’s constant

• This covers many failure modes of electronics
  
  *but not, for example, failures caused by mechanical fatigue*
Temperature, Test Time Relationship During Endurance Testing

\[ Stress \ Test \ Time \propto \frac{1}{Stress \ Temperature} \]

JEDEC Standard 218 uses the Arrhenius Equation in this form for calculations of temperature-accelerated stress times:

\[
t_S \left[ F H_S A e^{E_A/kT_{S,H}} + (1 - F H_S) A e^{E_A/kT_{S,L}} \right] \\
\leq t_U \left[ F H_U A e^{E_A/kT_{U,H}} + (1 - F H_U) A e^{E_A/kT_{U,L}} \right]
\]

Or to show the stress test time:

\[
t_S \leq t_U \frac{F H_U A e^{E_A/kT_{U,H}} + (1 - F H_U) A e^{E_A/kT_{U,L}}}{F H_S A e^{E_A/kT_{S,H}} + (1 - F H_S) A e^{E_A/kT_{S,L}}}
\]

\[ A = \text{constant scaling factor (this drops out of the calculations)} \]
\[ t = \text{time (in any units as long as all t values are in the same units)} \]
\[ T = \text{Temperature in } ^\circ \text{K} \]
\[ E_A = \text{Activation energy, assumed to be 1.1 eV} \]
\[ k = \text{Boltzmann's constant, 8.6171 \cdot 10^{-5} \text{ eV/} ^\circ \text{K}} \]
\[ F H = \text{Fraction of time spent at high temperature} \]
\[ S = \text{Subscript denoting the endurance stress itself} \]
\[ U = \text{Subscript denoting the use condition (enterprise vs. client)} \]
\[ H = \text{Subscript denoting the high temperature of interest} \]
\[ L = \text{Subscript denoting the low temperature of interest} \]
Endurance Acceptance Criteria

- **Sample size**
  Number of DUTs tested

- **Test Time and Temperature**
  TBW Rating must be met, with thermal acceleration
  If >1000 hrs, then we can use 1000 hrs test + extrapolation (per JESD218A)

- **Criteria (how many fails are allowed)**
  - FFR and UBER met with 60% statistical confidence
    \[
    UCL(\text{functional\_failures}) \leq FFR \times SS
    \]
    \[
    UCL(\text{data\_errors}) \leq \min(TBW, TBR) \times 8 \times 10^{12} \times UBER \times SS
    \]
  where
  - **FFR (Functional Failure Rate)** and **UBER (Uncorrectable Bit Error Rate)**
  - functional_failures is the acceptable number of functional failures
  - data_errors is the acceptable number of data errors
  - **TBW** is the endurance rating in terabytes written
  - **TBR** is the number of TB read
  - **SS** is the sample size in number of drives
  - UCL() is the upper confidence limit (used to determine # fails allowed)

- **For a zero-failure acceptance plan, UCL=0.92**

*From JESD218A*
Valuating Thermal Consistency

- In the range of typical 1000 hr RDT test:
  1°C = 100 hours test time

- Does this mean thermal consistency improvement of ±1°C ≈ 50 hours of test time?
  - No, unless your customer says so!
  - But a consistency of worse than ±5°C will require a longer test time, lower UCL, or invalidate test results

- JEDEC spec is based on ±5 °C
  “The apparatus required for this test shall consist of a controlled temperature chamber capable of maintaining the specified temperature conditions to within ±5 °C”
  - JESD218A Section 8.1

<table>
<thead>
<tr>
<th>Actual endurance stress hours</th>
<th>Temperature (°C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>700</td>
<td>85°C</td>
</tr>
<tr>
<td>800</td>
<td>83°C</td>
</tr>
<tr>
<td>900</td>
<td>82°C</td>
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<tr>
<td>1000</td>
<td>81°C</td>
</tr>
<tr>
<td>1200</td>
<td>79°C</td>
</tr>
<tr>
<td>1400</td>
<td>78°C</td>
</tr>
</tbody>
</table>

From JESD218A Table 4

- If reaching TBW rating takes \( \gg 1000 \) hrs, then 1000 hrs. plus extrapolation is still used
Why Thermal Consistency is Important

• Maintain quality with manufacturing consistency
  • Inconsistent thermal conditions create potentially unrepeatable test results for SSDs
    and headaches for SSD Engineers

• Meet conditions for Reliability Demonstration Tests
  • JEDEC specifies ±5 °C for test equipment*
    * Actual conditions determined by manufacturer and customer/buyer:
      “Alternative requirements and acceptance criteria are up to the manufacturer and purchaser to agree upon.” –JESD218A

• Violating thermal consistency requirements during a Qual → might mean starting over!
  • Longer time to market = less market share, lower margins
Factors Affecting Thermal Consistency in Multiple DUT Chamber

• Chamber Performance Factors
  • Total air flow and temperature
  • Air guides and baffles
  • DUT count, locations, and spacing

• DUT power consumption
  • Power generated = heat; heat must be removed
  • Worst case is with all DUTs at full power
  • New PCIe 3.0 DUTs can be 25W compared to <10W for SATA
Multi-DUT Chamber Considerations

DUT Spacing

• DUTs positioning perpendicular to airflow
  • Too close: thermal disturbance between DUTs
  • Too far apart: more expensive (floorspace)
  • Need to balance spacing with airflow and air temperature

• DUT positioning inline with air flow
  • A gradient in temperature will occur
  • Need to balance airflow and number of DUTs in series
Multi-DUT Chamber Considerations

Vertical Positioning

- Airflow loops through chamber to the compressor
- Baffles are needed to guide air into the chamber evenly
- Here is one scenario for 25W DUTs to meet ±5°C
  - 4 levels per chamber
  - 8 DUTs deep
  - 4 DUTs long

*Note: two chambers per 256 DUT system*

Poor baffling or too many vertical layers in a single chamber causes vertical temperature gradient
Things We Can Control
Airflow Consistency: Baffles, Empty Sockets

- **Fluid dynamics of air flow for electronics:**
  \[ \text{Pressure (V)} = \text{Air Flow (I)} \times \text{Wind Resistance (R)} \]

  - Empty inline air channel = inconsistent airflow
  - Empty perpendicular air channel = OK
  - Empty space between trays = inconsistent airflow
  - Baffles restrict air flow (e.g. half-height vs. full-height cards)
Multi-DUT Thermal Chamber Design

- Air flow is complex,
  - Sophisticated simulation, including baffles and DUT form factors is necessary to aid chamber design including baffles and DUT form factors

Thermal chamber airflow simulation
DUT Power Effects

Measurement Setup

- Two chambers with 128 DUTs each
  - 4 DUTs in line with air flow, 8 DUTs deep, 8 DUTs high
- Resistor/thermal sensor “DUTs”
  - Form Factor ≈ HHHL PC Card
  - Control power output of resistor to simulate DUT power
- Airflow, baffles, set to achieve ±5°C with full load of 256 DUTs x 25W = 6.4kW
  - Airflow between 1100 lfm and 1700 lfm
- Set point does not affect consistency (within operating range)
  - Set point is the air temp, device temp is much higher

2 trays each with 2 rows of 8 DUTs

Test DUT with resistor and thermal sensor
DUT Power vs. Thermal Consistency

- 256 @0W +/-1.1°C
- 128 @10W +/- 1.5°C
- 256 @12W +/- 3.6°C
- 256 @25W +/- 5.0°C

Set point does not affect consistency (in operating range)
Set point is air temp, device temp is much higher

256 DUTs at 25W, 6.4kW total at ±5°C

128 DUTs at 10W, 6.4kW total at ±1.5°C
Summary

- DUT power consumption poses thermal challenges to test
  - High-wattage PCIe SSDs can consume 4-5x power of previous SATA SSDs
    - Lower DUT power will have better thermal consistency
  - Thermal consistency suffers, affecting endurance test parameters
  - Cooling must accommodate higher power devices to prevent thermal runaway
  - Thermal chamber design and usage is critical to meeting test criteria

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