

RRAM Opportunity for High density memory application

6. Aug. 2014

SuOck Chung

SK hynix R&D Div.

Emerging devices

- . Wearable
- . Automotive
- . Mobile health-care
- . IoT

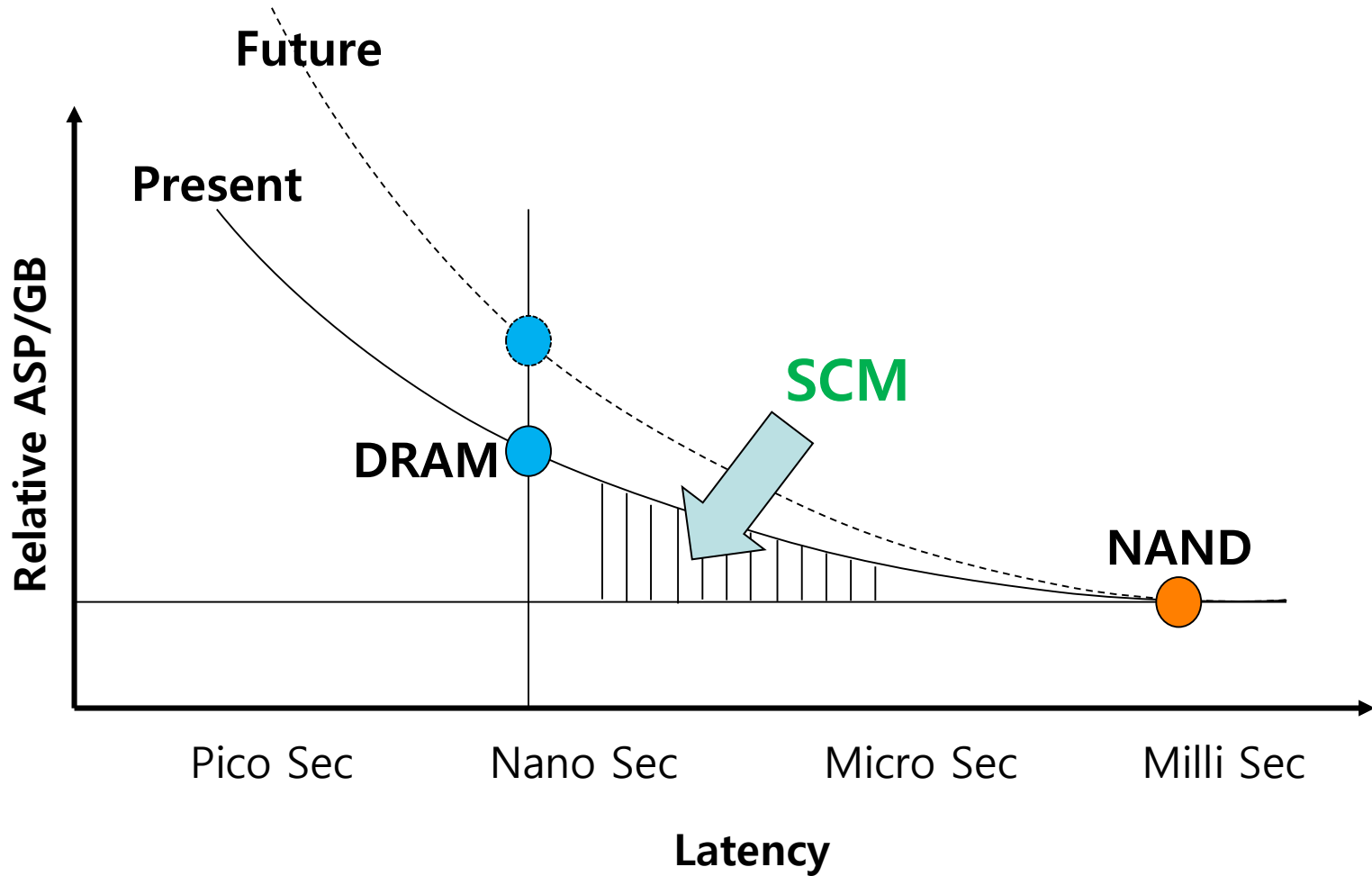
Cloud
Big data
Virtualize
Network



New computing system

- . Exascale
 - . Multi-cores
 - . **New memory technology**
 - Byte accessibility
 - Capacity ?
 - Latency ?
 - Bandwidth / power ?
 - Endurance ?
- ➔ **SCM**

Gap b/w DRAM ~ NAND



RRAM Potentials

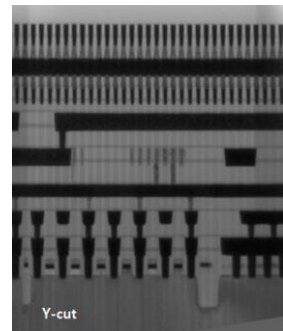
←Low Risk high→ ● ● ● ●	DRAM	NAND	PRAM (SLC)	STTRAM	RRAM (TMO)	RRAM (CBRAM)
Byte-Accessible	●	●	●	●	●	●
Write Latency	●	●	●	●	●	●
Write Bandwidth	●	●	●	●	●	●
Endurance	●	●	●	●	●	●
Data Retention	●	●	●	●	●	●
Power / Bandwidth	●	●	●	●	●	●
3D Solution	●	●	●	●	●	●
Bit Density (Cost)	●	●	●	●	●	●
Manufacturability	●	●	●	●	●	●

- **Requirements for SCM**

- Non-volatile, byte accessible
- High capacity + Short latency + Wide B/W @ moderate power

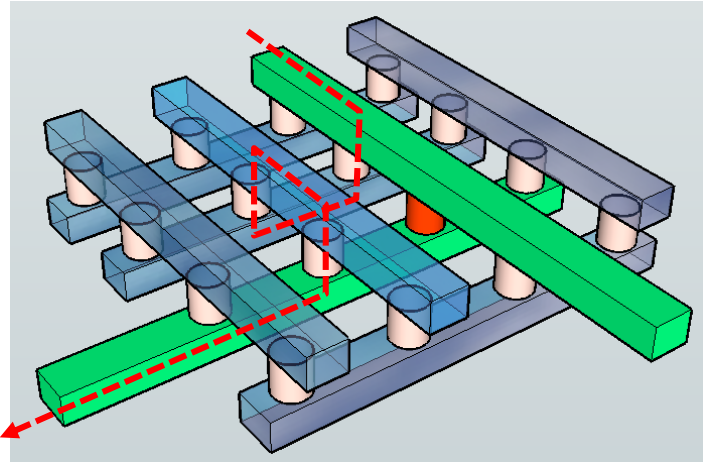
- **ReRAM is a good candidate**

- Smaller power consumption than PRAM ($I_{reset} < 1/3$)
- Cross Point Array (XPA) + Multi-Level Stacking (MLS)



Major challenges

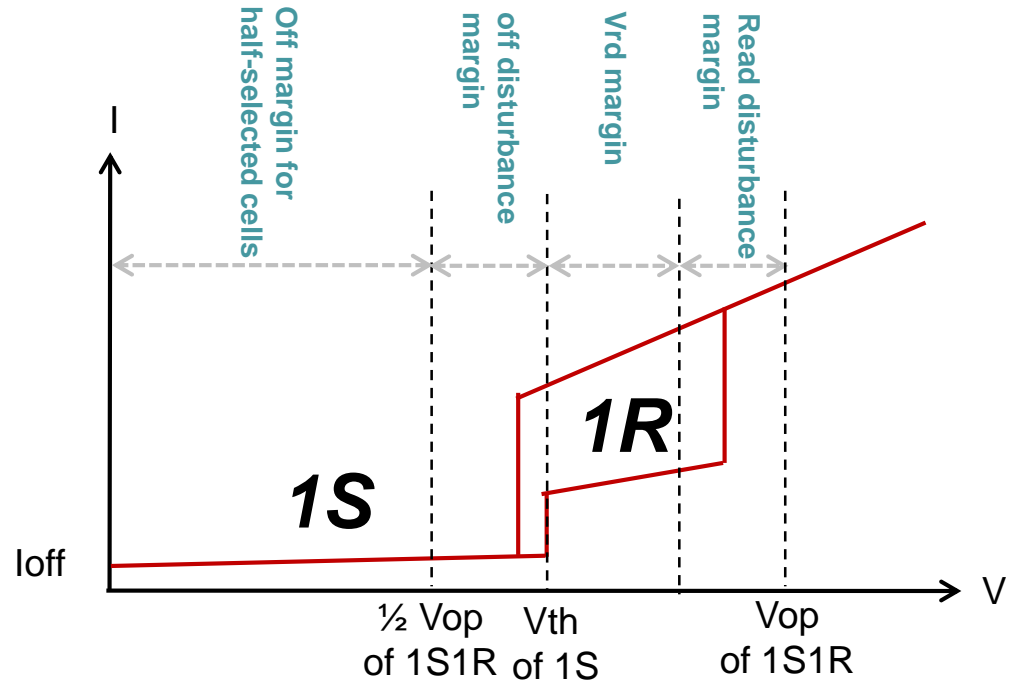
Sneak current effect



 Selected cell  Sneak path

- Originated from imperfect off
- Large operation power,
Sensing noise issue
- Non-linear 1R → 1S1R
Lower the I_{off} of 1S

2 Terminal Operation (1S+1R)



- Simple process merit
- Narrow data window
→ Good match of 1R+1S I-V
→ Higher V_{op} ?

Summary

- Recent ICT tech trend requires SCM type memory (high capacity + shorter latency + smaller power). RRAM is an attractive candidate for SCM.
- SK hynix has explored and developed core technologies (especially, cell and array architecture) for RRAM production.
- Stackable selector's I_{off} and cell data window are key success factors for high density RRAM product.