



**devicepros**

## HW Acceleration of Memcached

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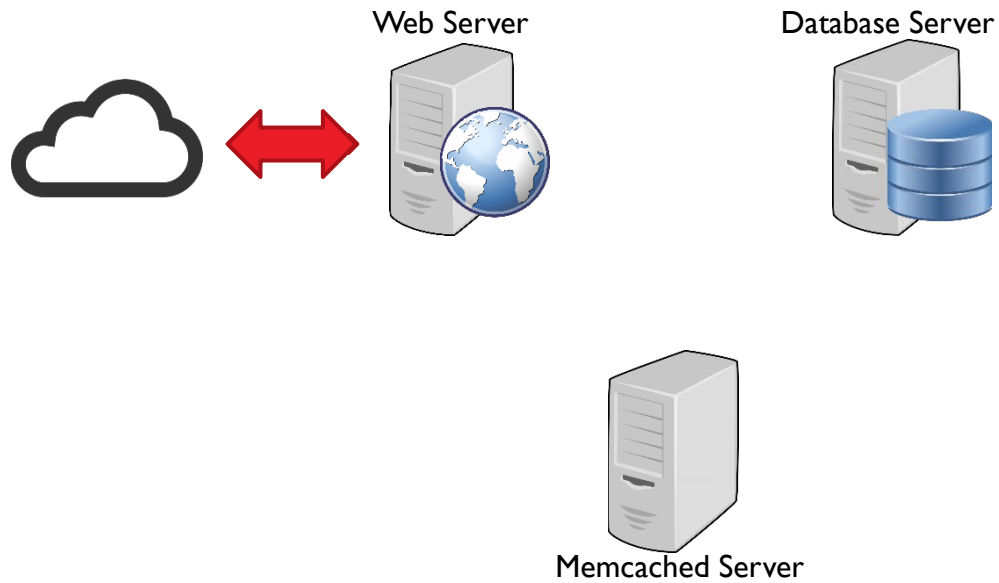
# Agenda

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- ▶ Quick introduction to Memcached
- ▶ Scaling Memcached as a software solution
- ▶ Performance and some use cases
- ▶ A Memcached server on FPGA

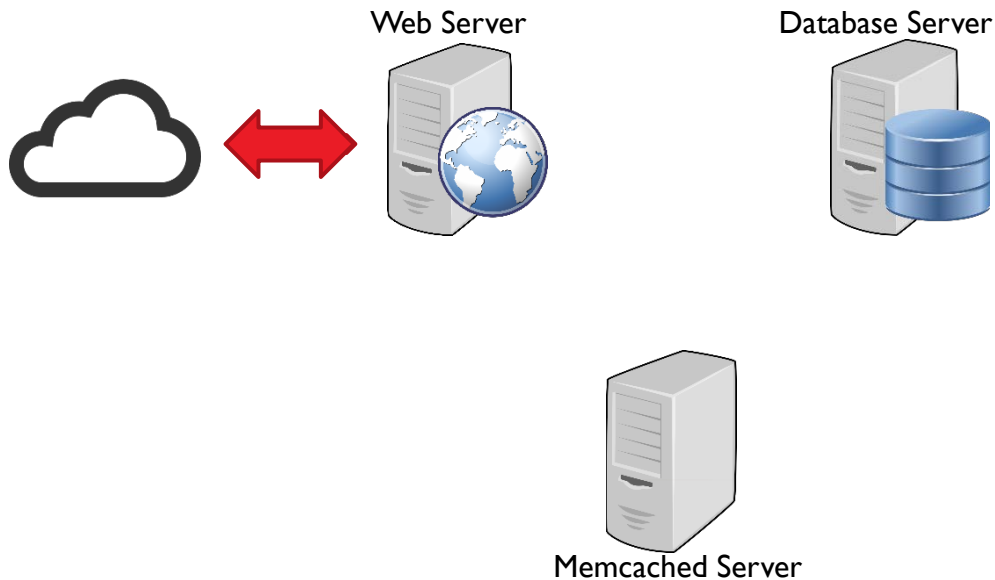
# How Memcached is used

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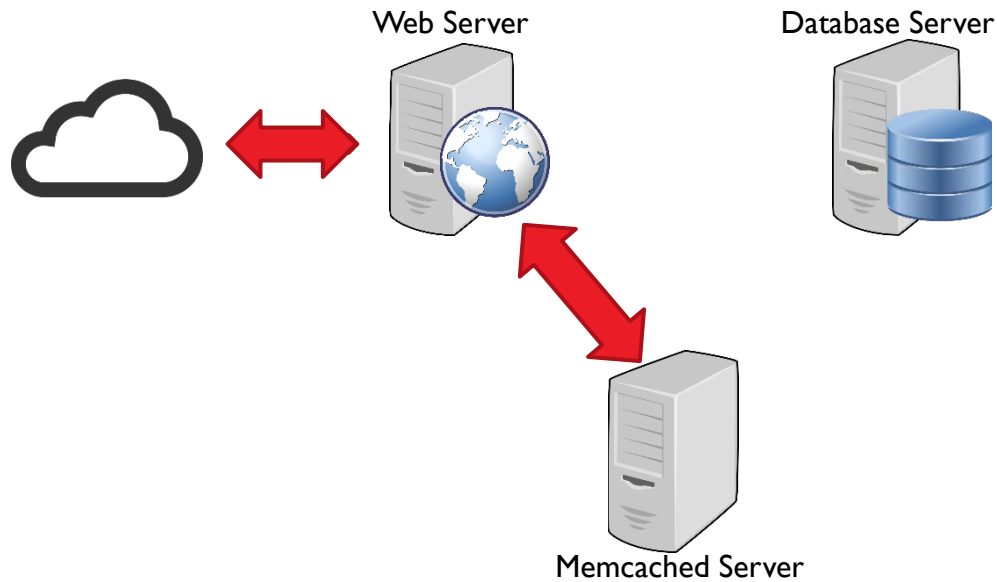
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function get_foo(foo_id)
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  foo = memcached_get("foo:" . foo_id)  
  return foo if defined foo
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  foo = fetch_foo_from_database(foo_id)  
  memcached_set("foo:" . foo_id, foo)  
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end
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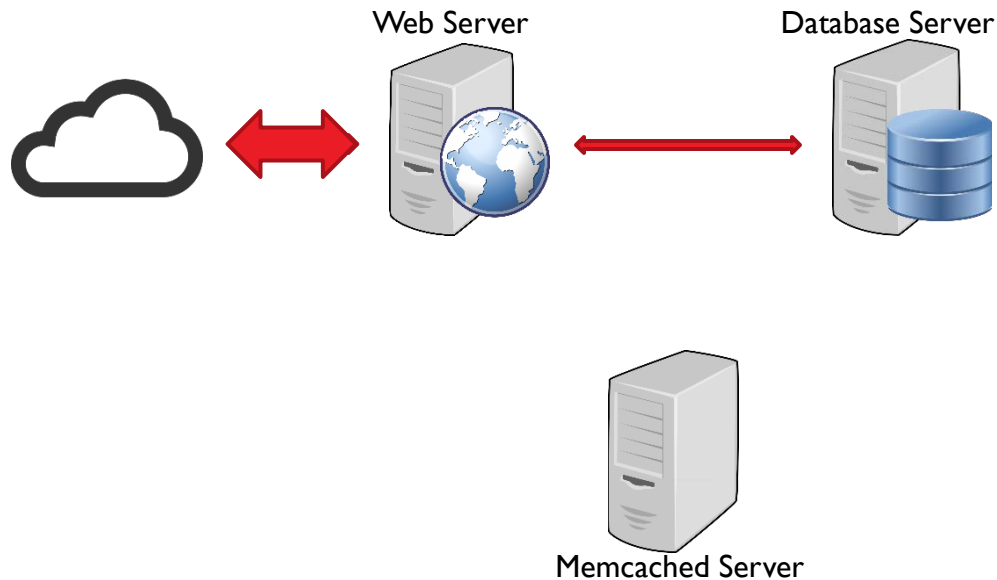
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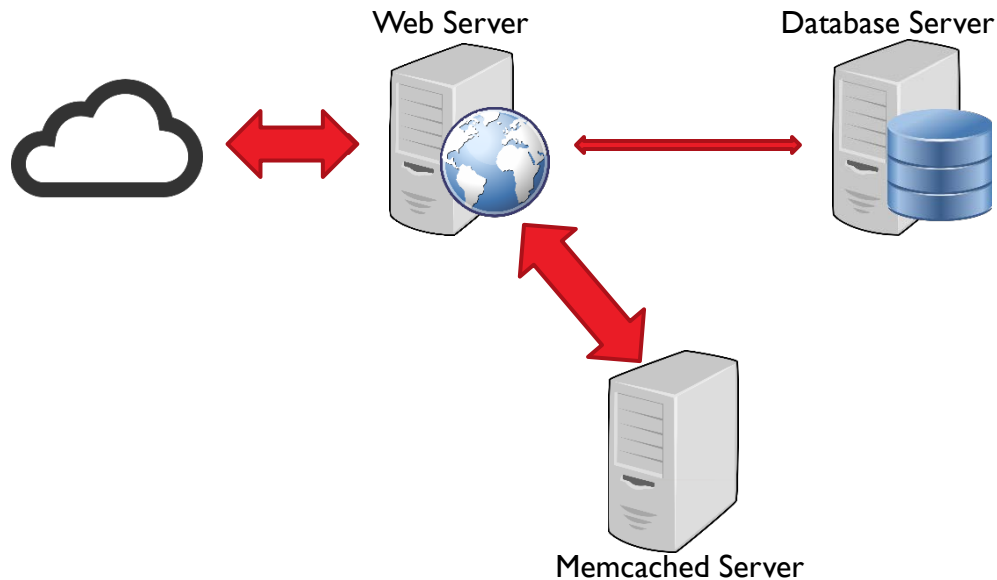
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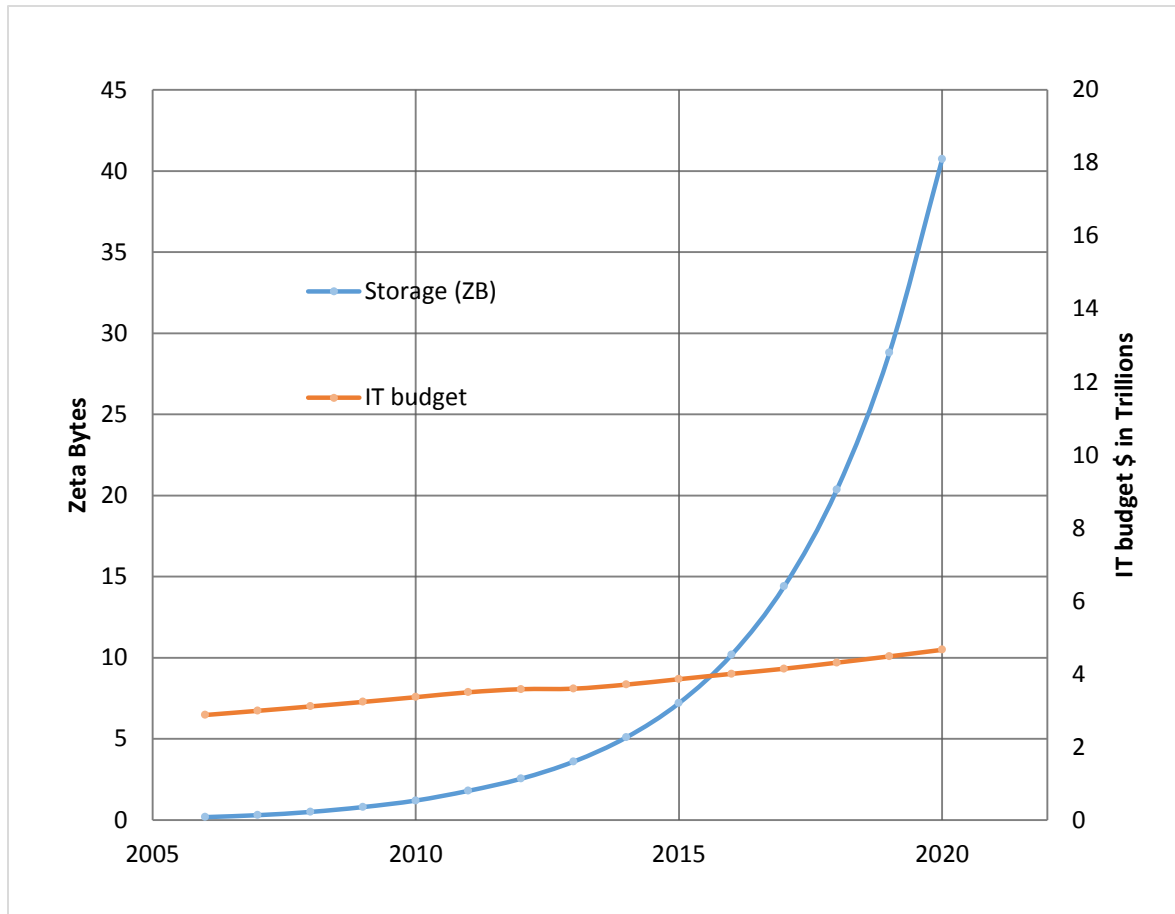
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# Universe of Data growth vs. IT budgets



## Growth by 2020

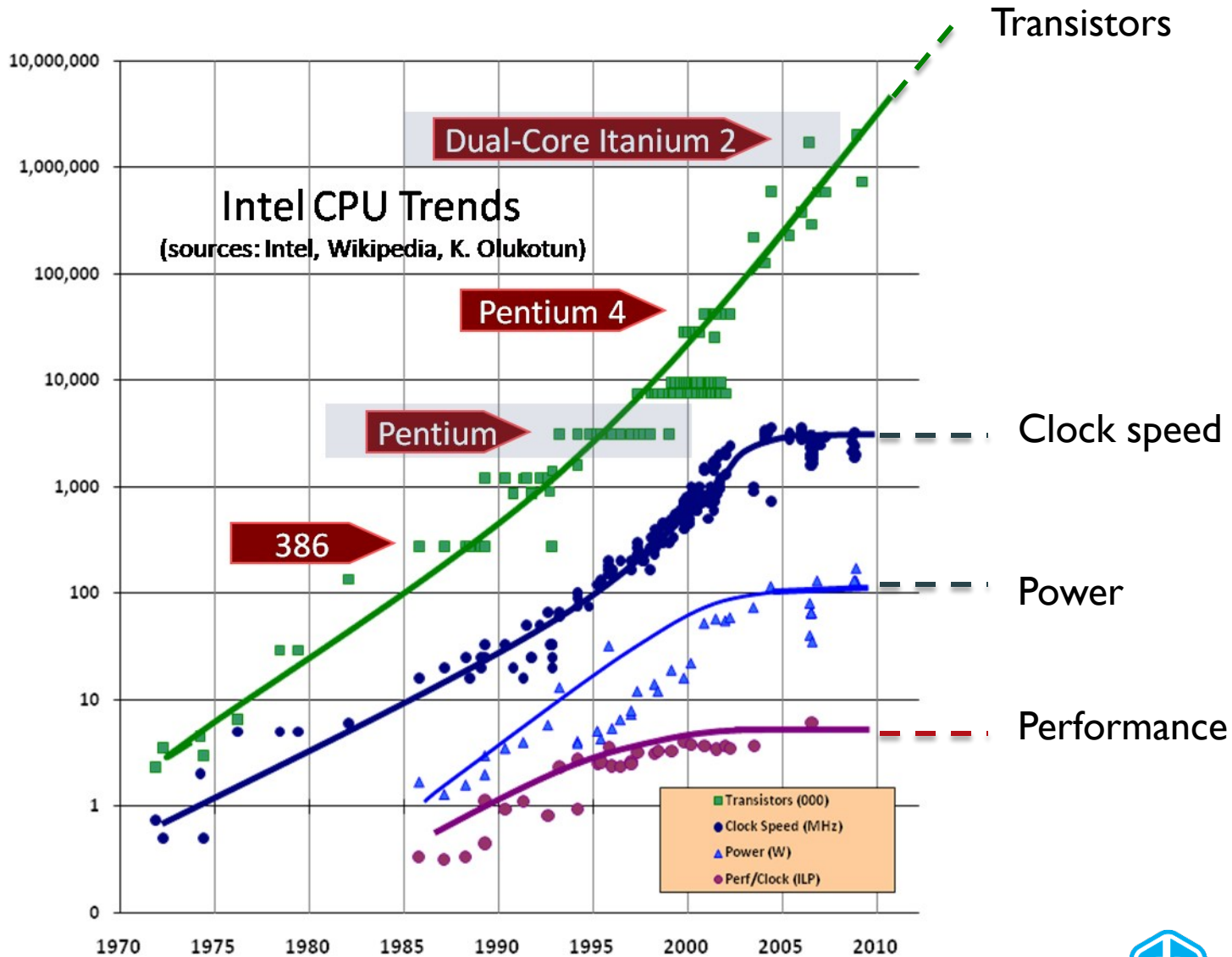
- 14X Enterprise data
- 10X Servers
- vs. 1.5X IT professionals

Memcached accounts for  
10-30% of servers

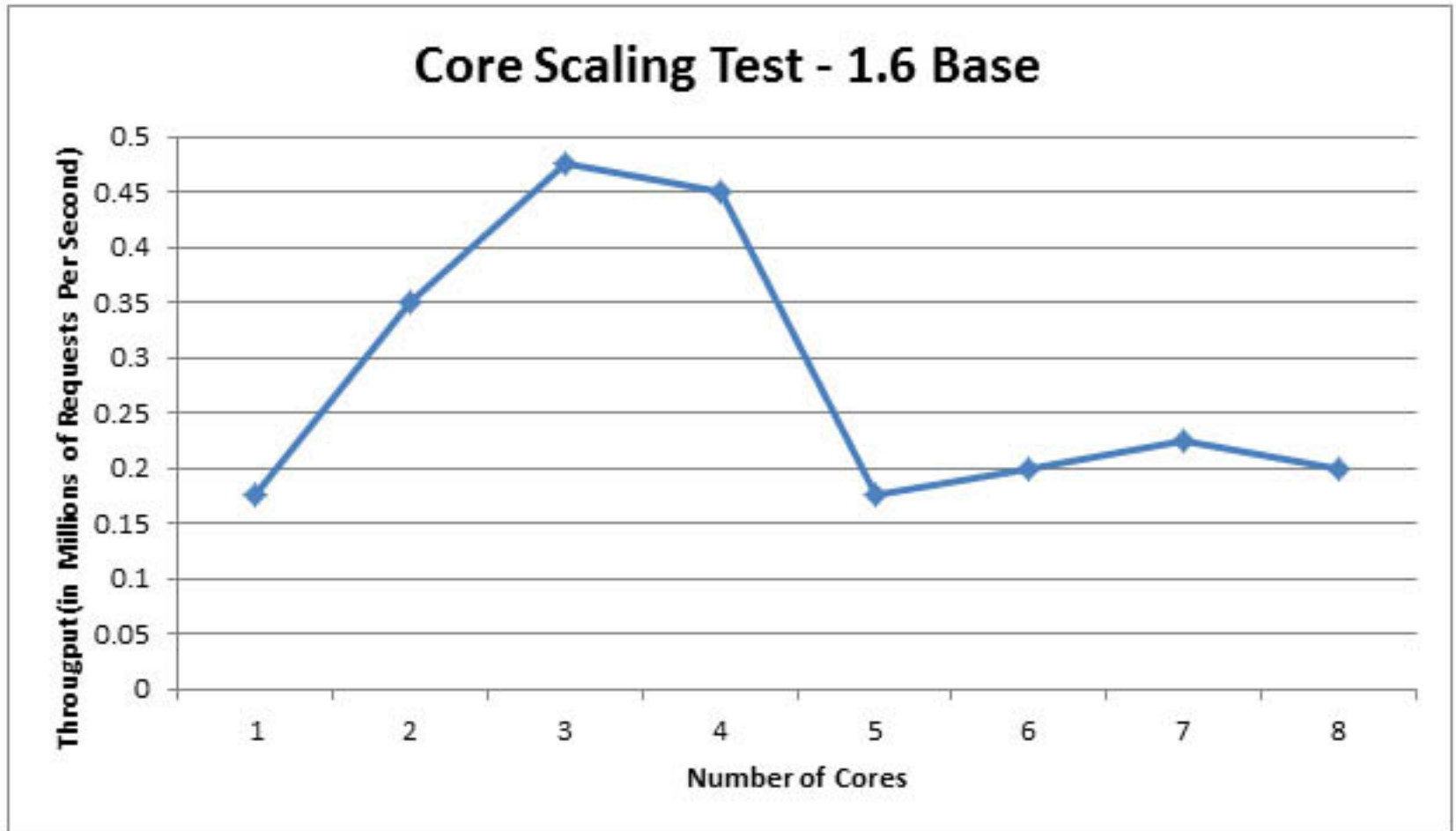
IDC Digital Universe Study



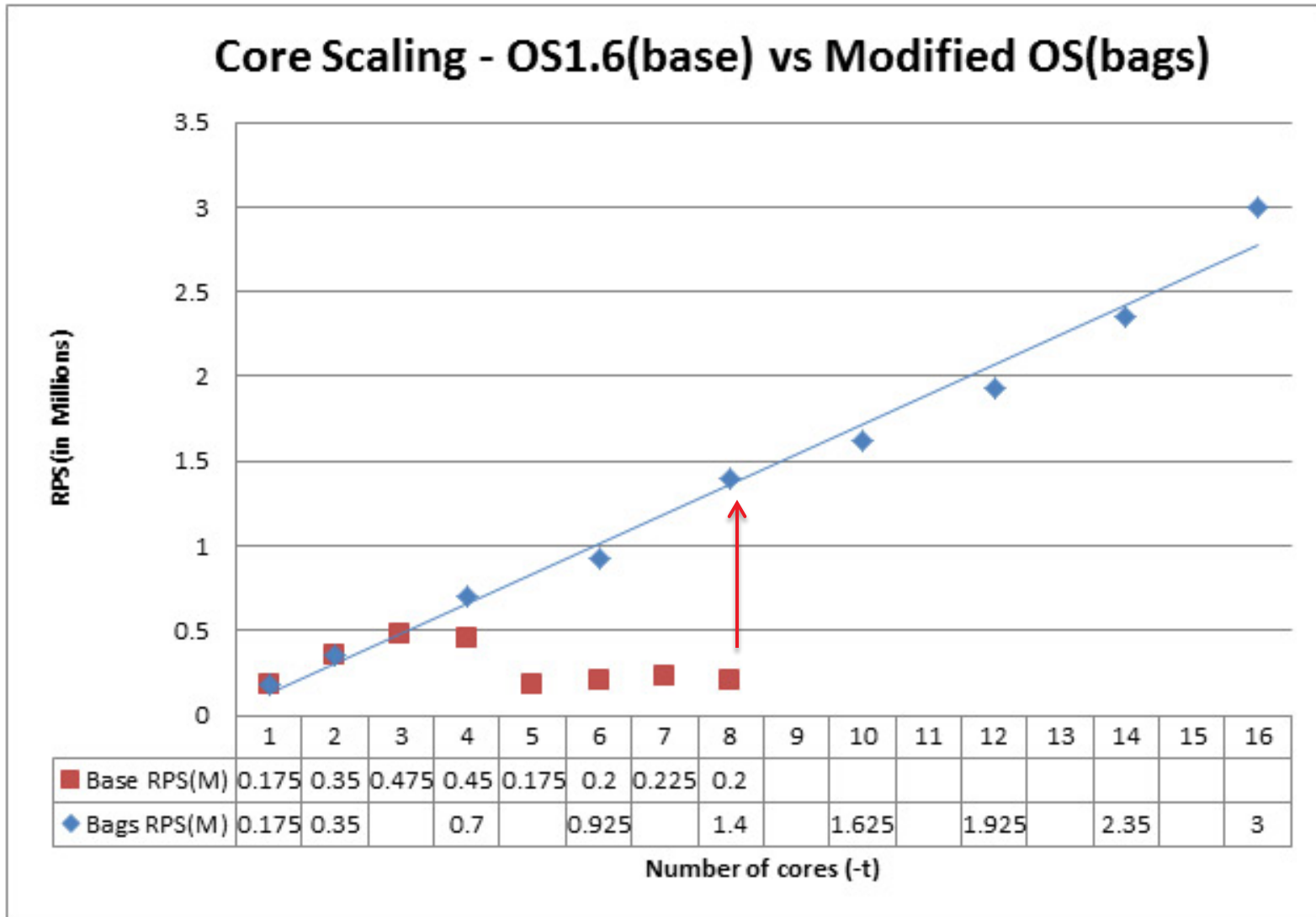
# Intel CPU Trends



# Intel 2012 Paper on Memcached scalability

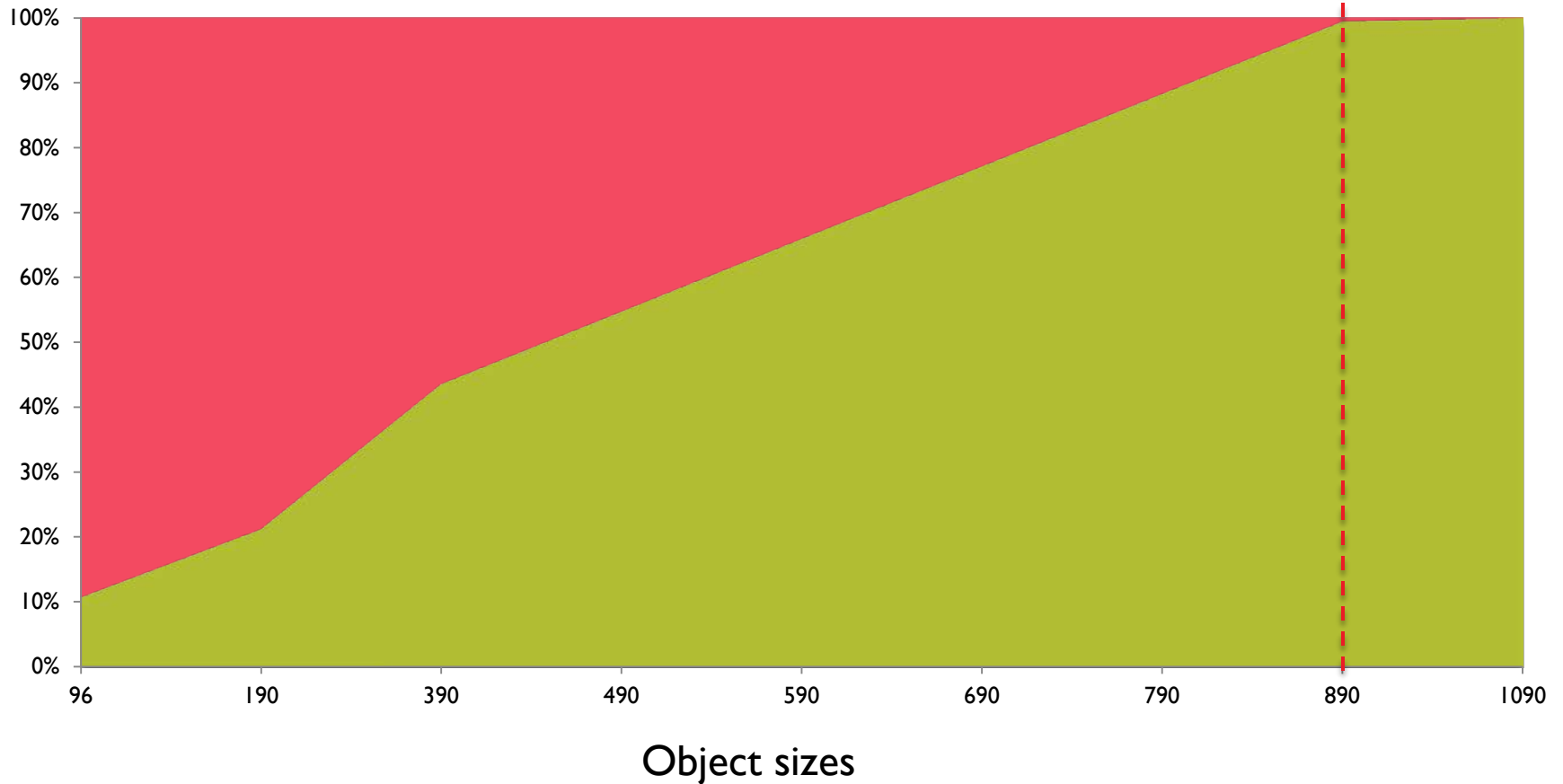


# Intel 2012 Paper on Memcached scalability



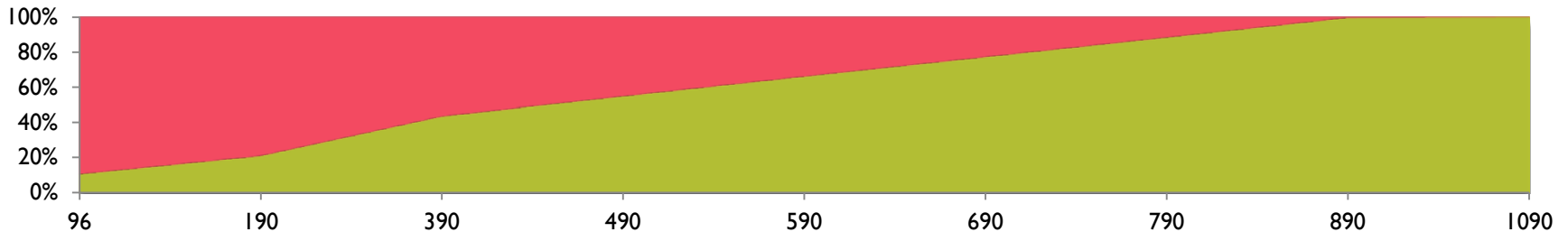
# Network not saturated for small Object sizes

## 10GbE Saturation (8 cores)



# Network not saturated for small Object sizes

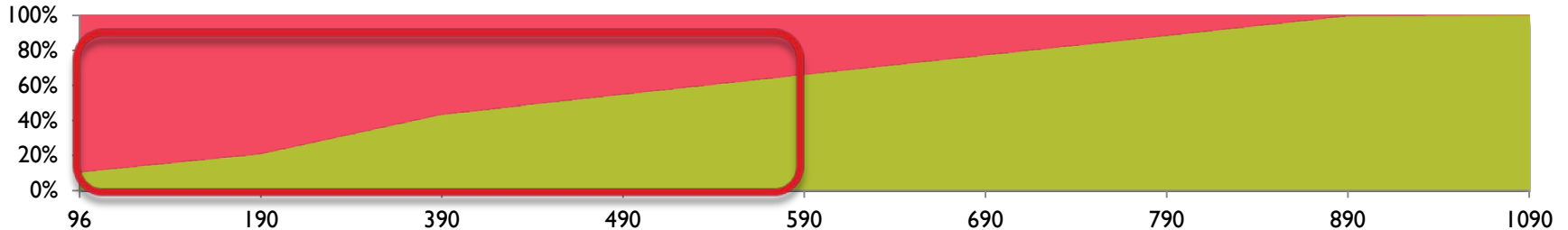
## 10GbE Saturation (8 cores)



Calculated probability of value sizes									
Value size [Bytes]	128	256	512	768	1014	2048	4096	22000	32000
Facebook: ETC	0.55	0.075	0.285	0.015	0.025	0.025	0.025	0	0
Facebook: USR	1	0	0	0	0	0	0	0	0
Facebook: APP	0.12	0	0.63	0.21	0.03	0.01	0	0	0
Facebook: VAR	0.78	0.02	0.17	0.03	0	0	0	0	0
Twitter	0	0	0	0.1	0.85	0.05	0	0	0
Wiki	0	0	0	0	0.58	0.02	0.1	0.25	0.05
Flicker	0	0	0	0	0	0	0	0.1	0.9
Youtube	0	0	0	0	0	0.75	0.11	0.11	

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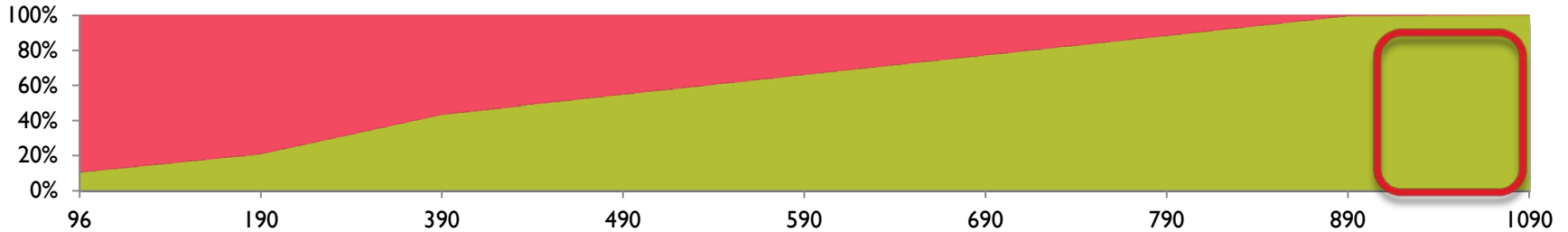


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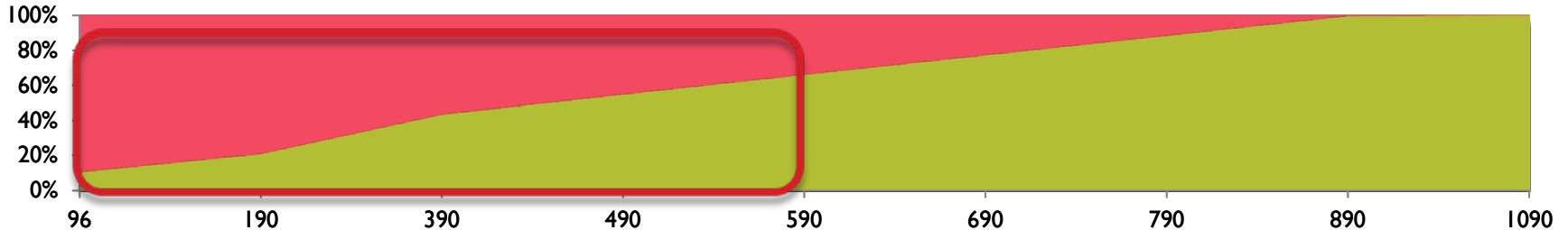
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# Network not saturated for small Object sizes

100Gbps Saturation (16 cores)



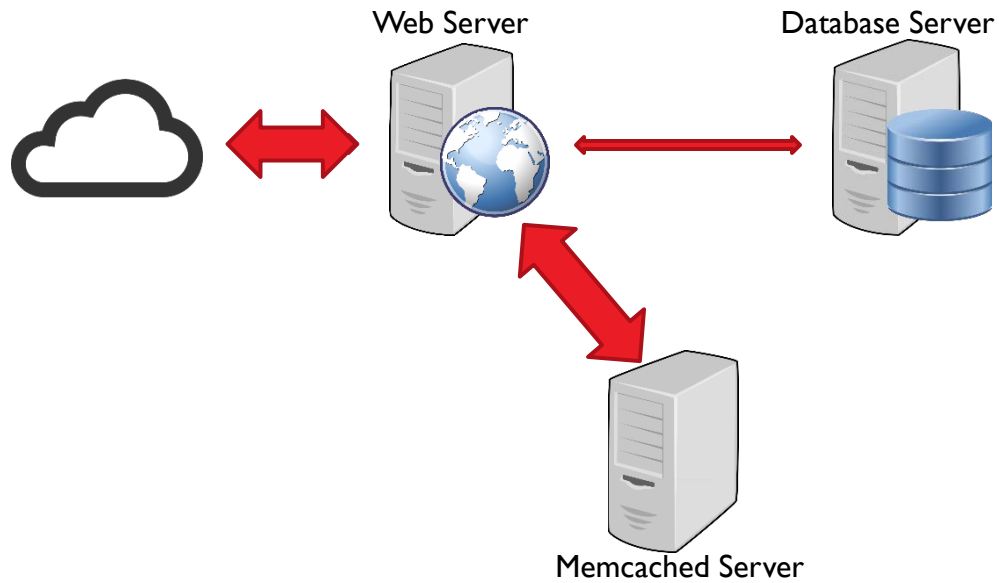
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Value size [Bytes]	128	256	512	768	1014	2048	4096	22000	32000
Facebook: ETC	0.55	0.075	0.285	0.015	0.025	0.025	0.025	0	0
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Flicker	0	0	0	0	0	0	0	0.1	0.9
Youtube	0	0	0	0	0	0.75	0.11	0.11	

How would this look with 16 cores?



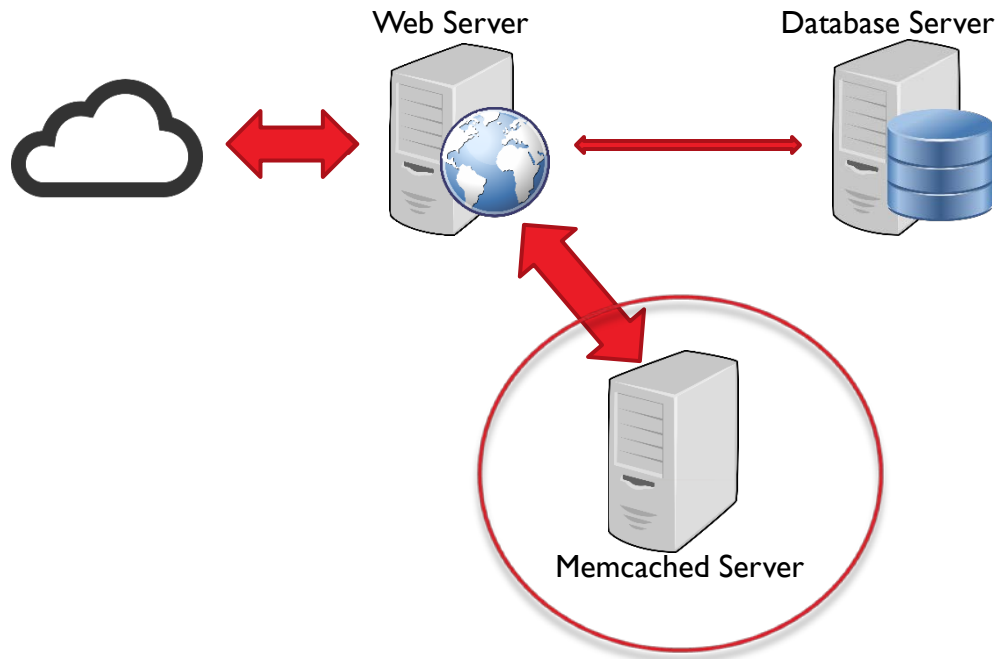
# Memcached

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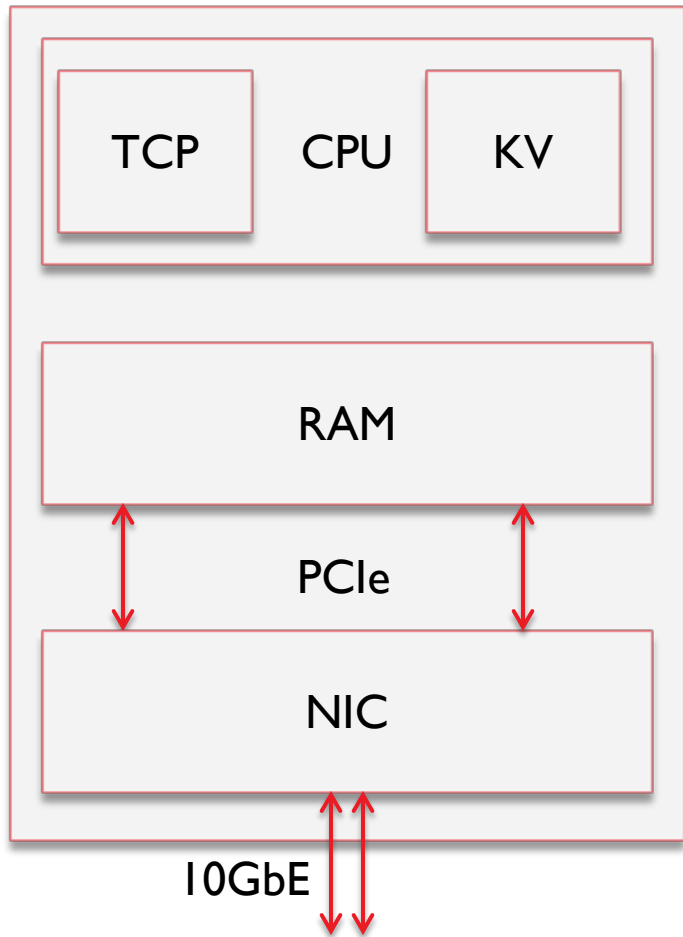
# Memcached

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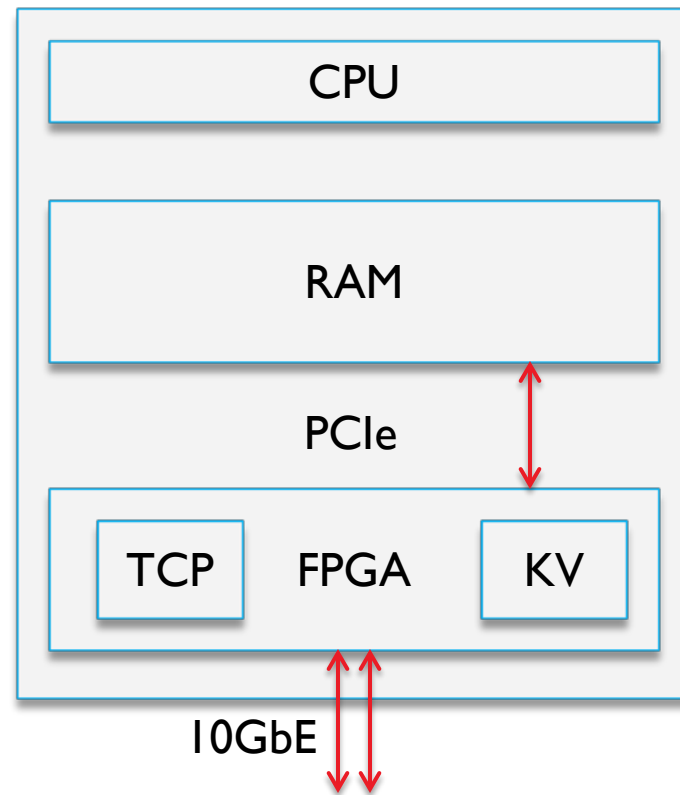
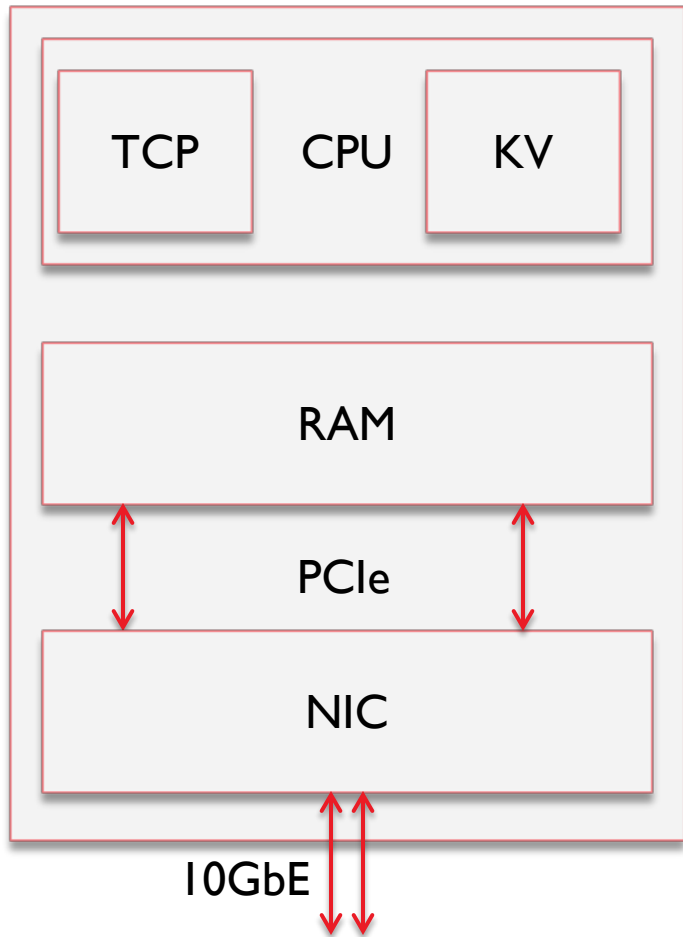


# High Level View of Software Approach

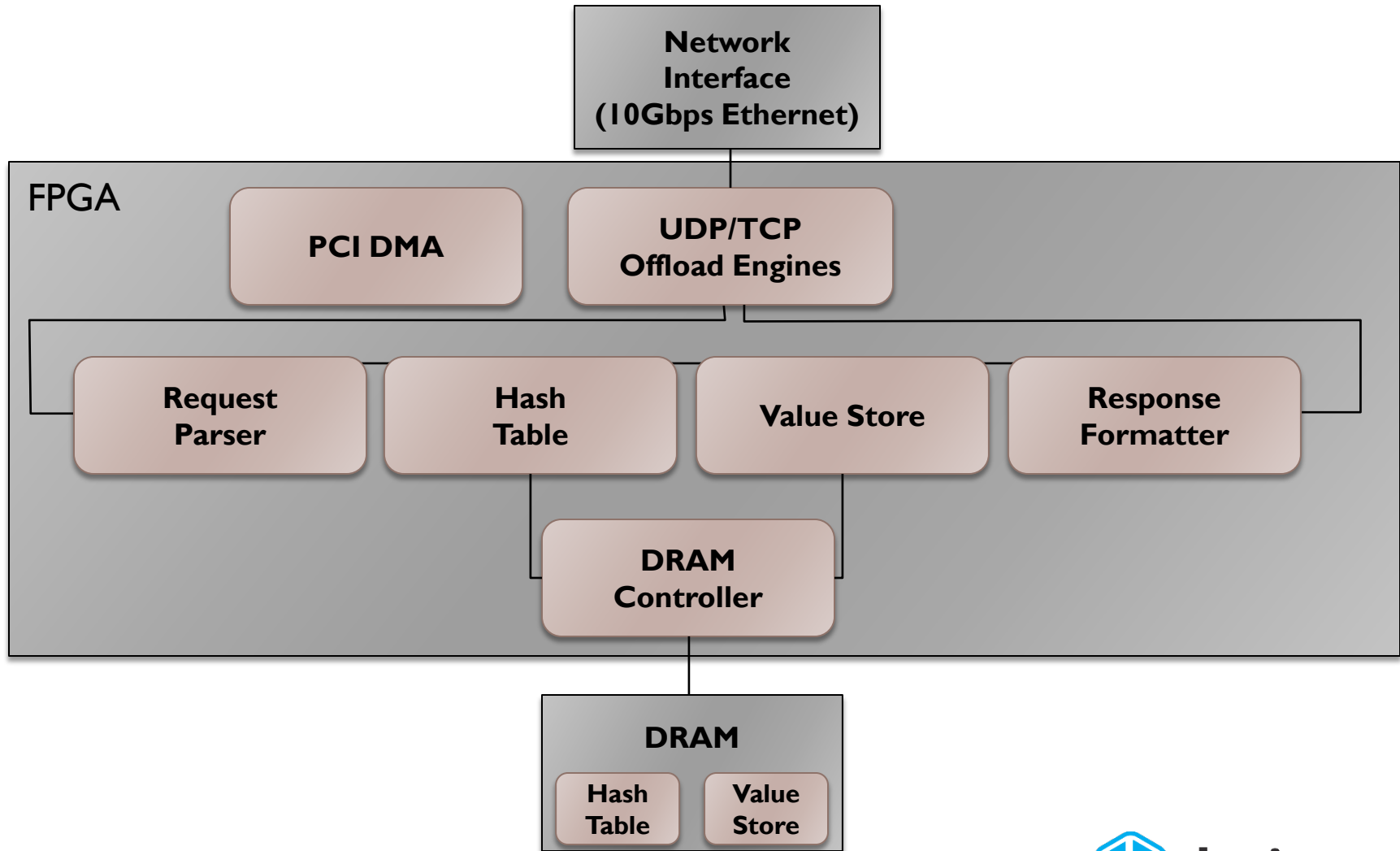
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# Alternative approach with FPGA

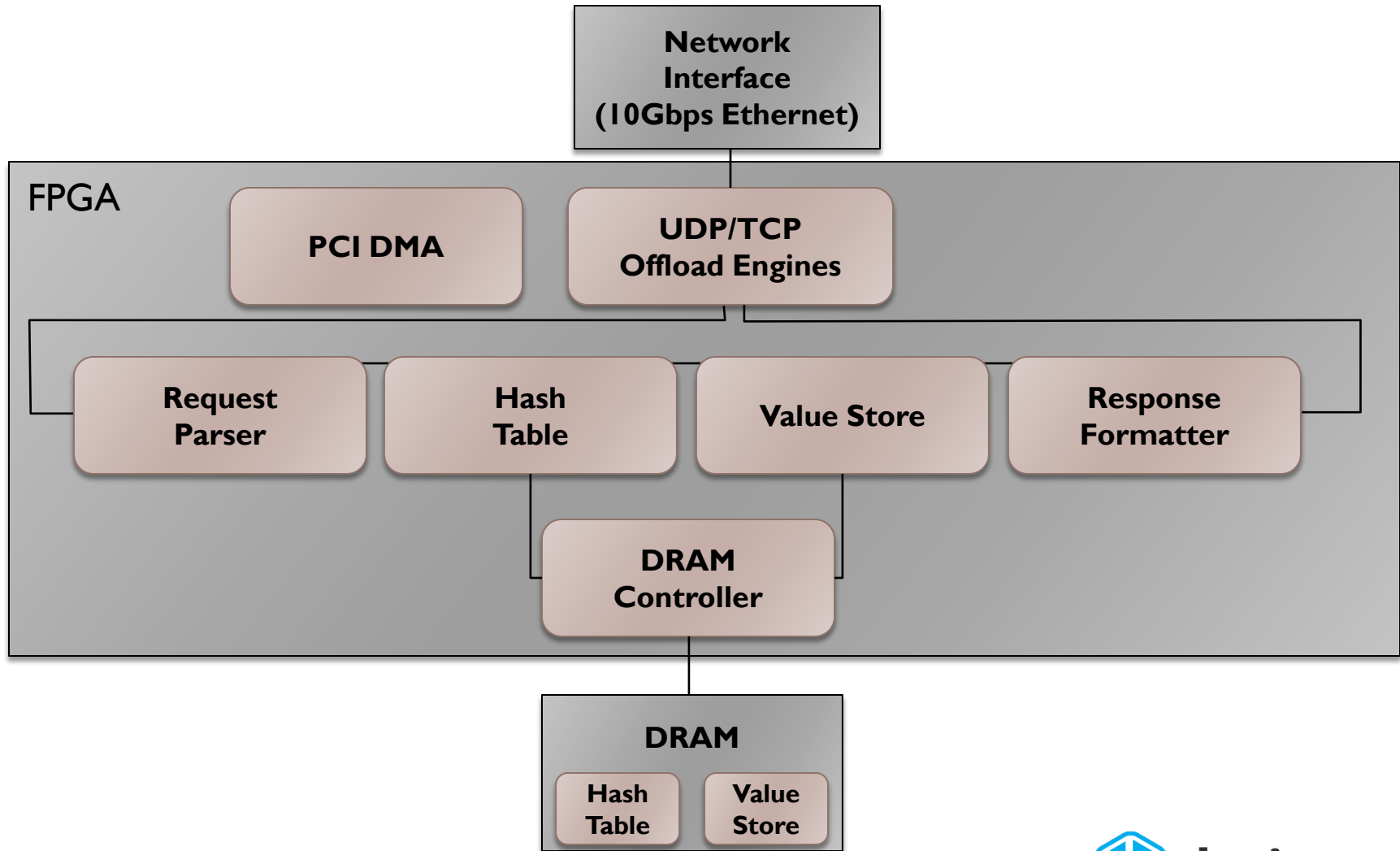


# Xilinx Memcached processing pipeline



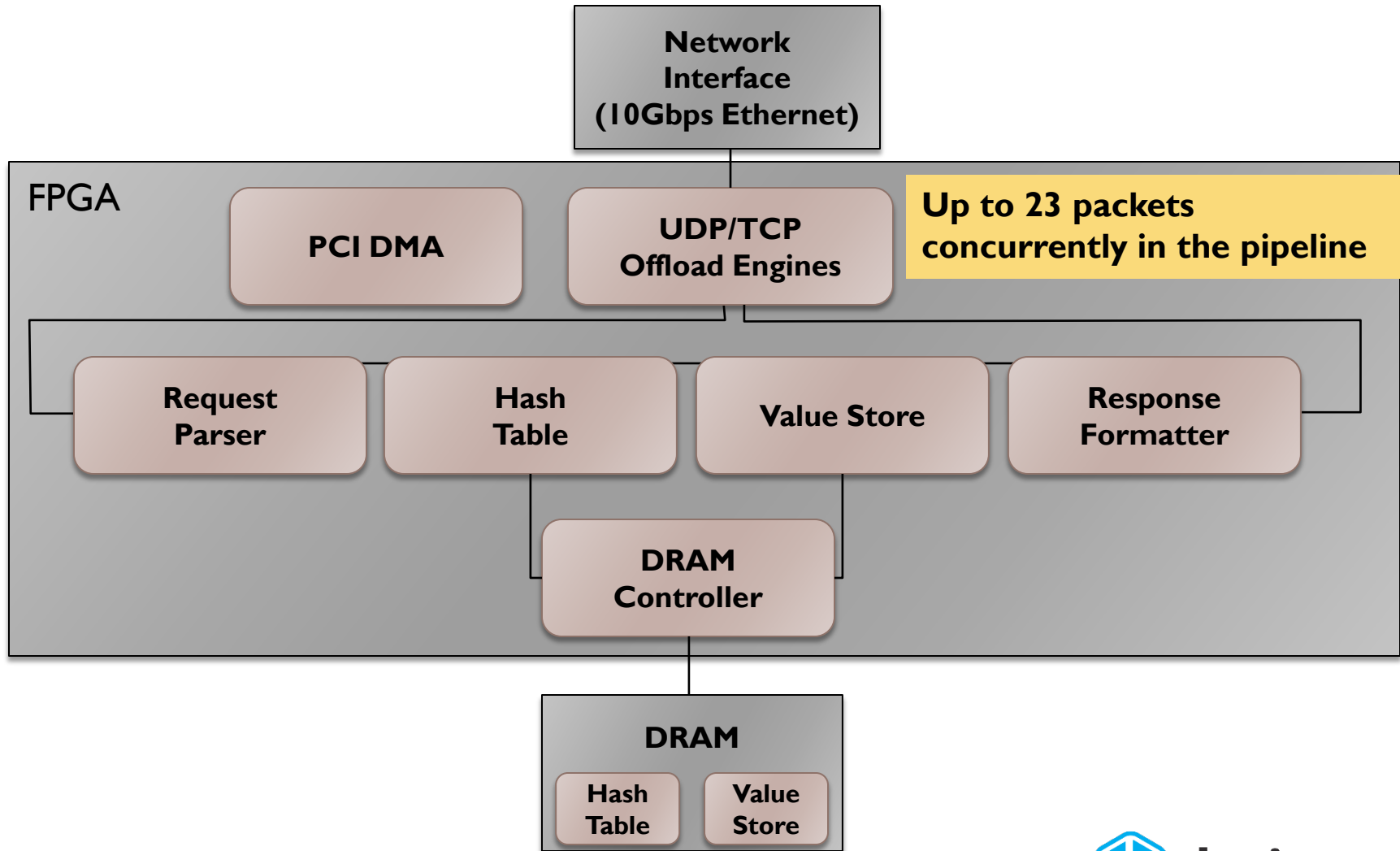
# Xilinx Memcached processing pipeline

481 cycles @ 156MHz vs. 0.5-1 Million cycles @ 2GHz



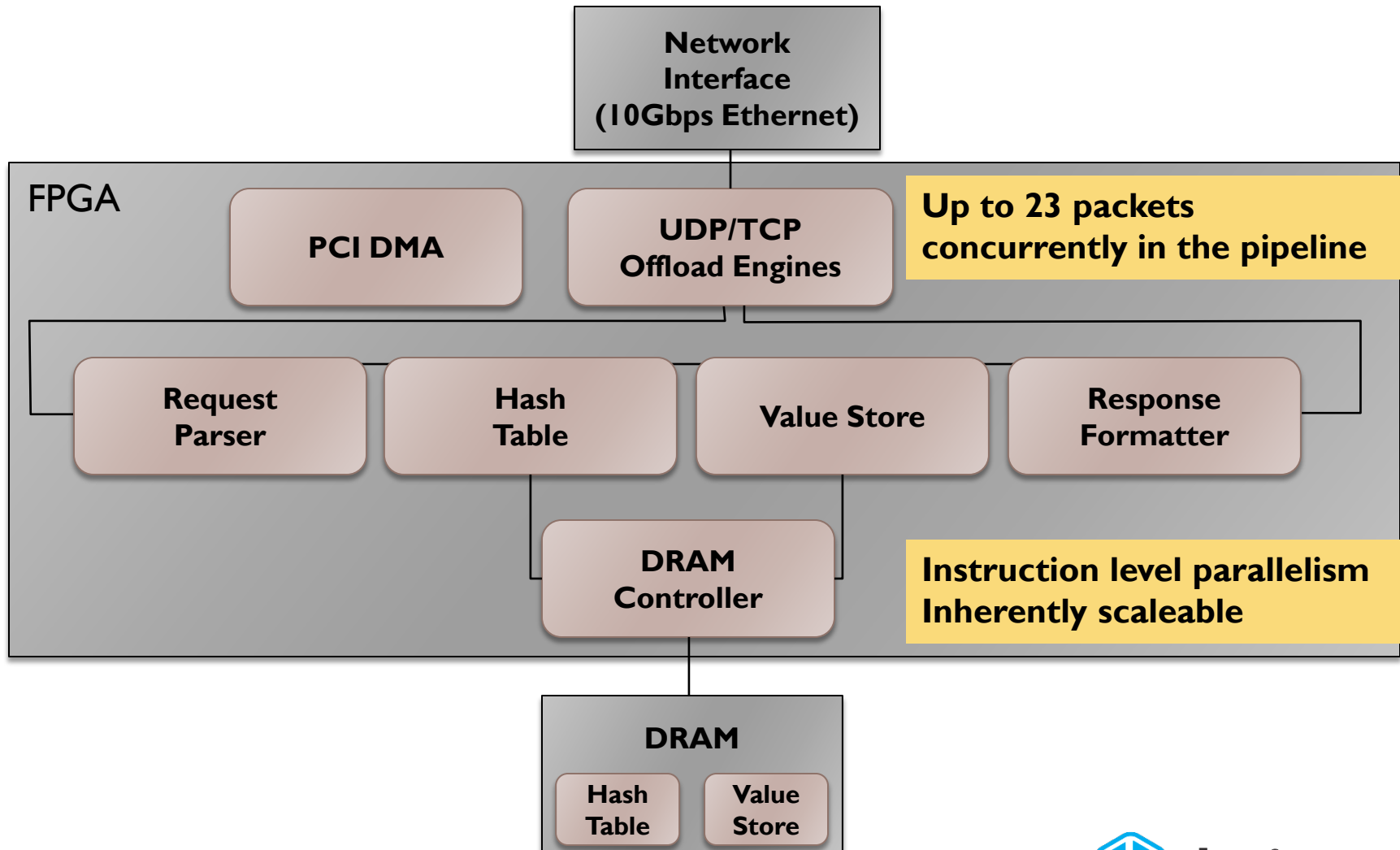
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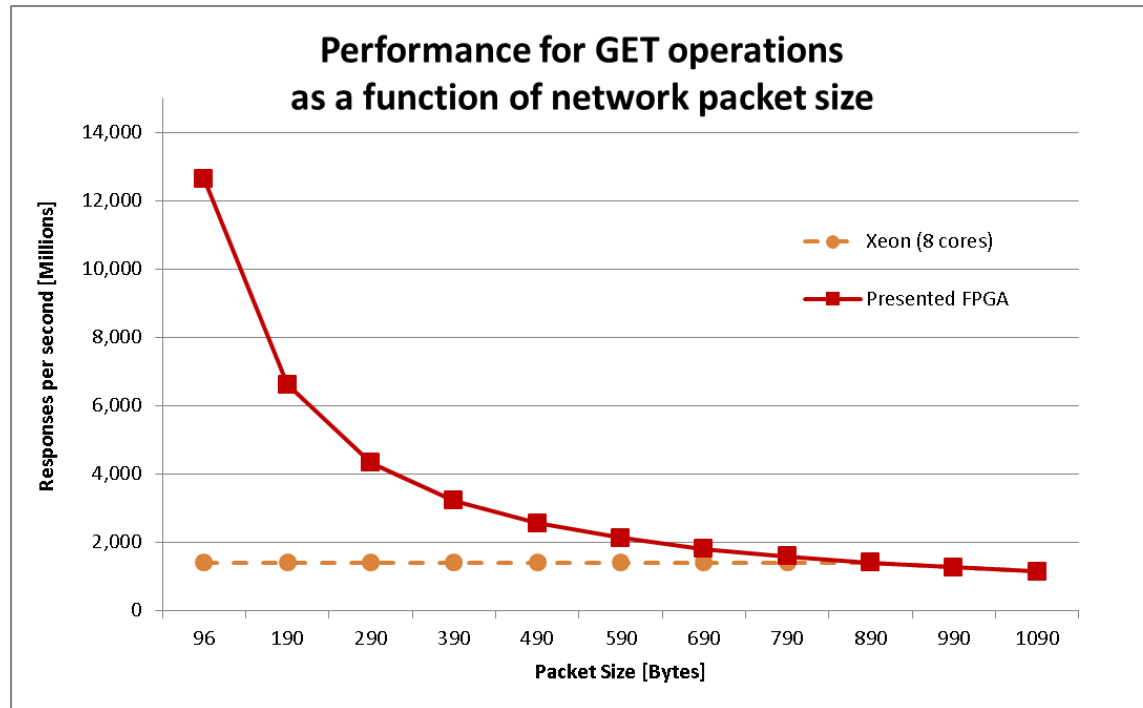
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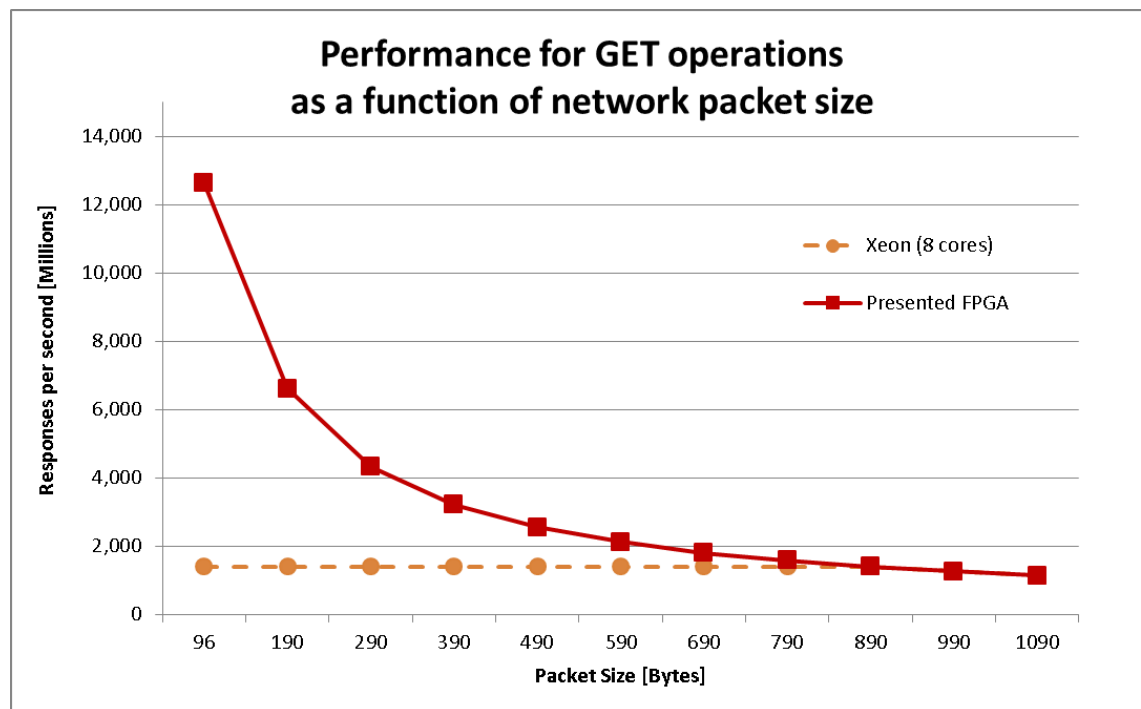




# FPGA vs. Xeon 8 core with tuned Memcached



# FPGA vs. Xeon 8 core with tuned Memcached



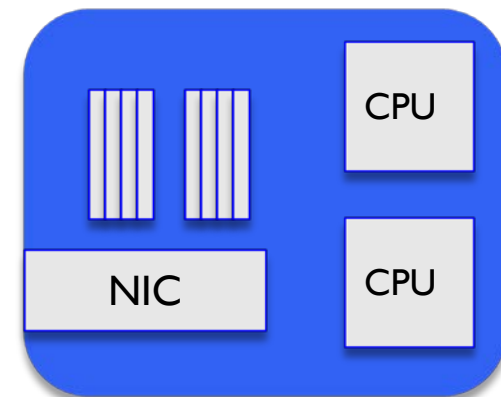
Platform	RPS [M]	Latency [us]	RPS/W [K]
Intel Xeon (8 cores)	1.34	200-300	7
FPGA (board only)	Up to 13.02	3.5-4.5	254.8
FPGA (with host)	Up to 13.02	3.5-4.5	106.7

# Memcached server cost, power, performance

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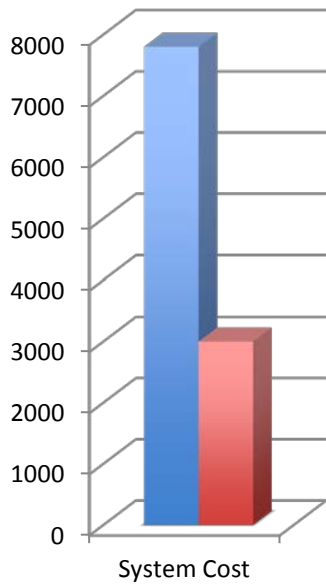


Agoraic Solution



Intel Dual Xeon

# Memcached server cost, power, performance

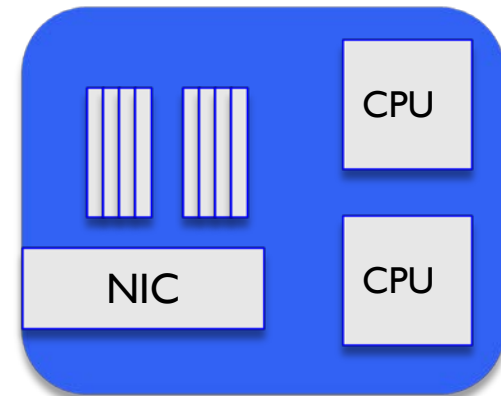


■ Dual Intel Xeon ■ Agoraic

**60% lower**  
System Cost

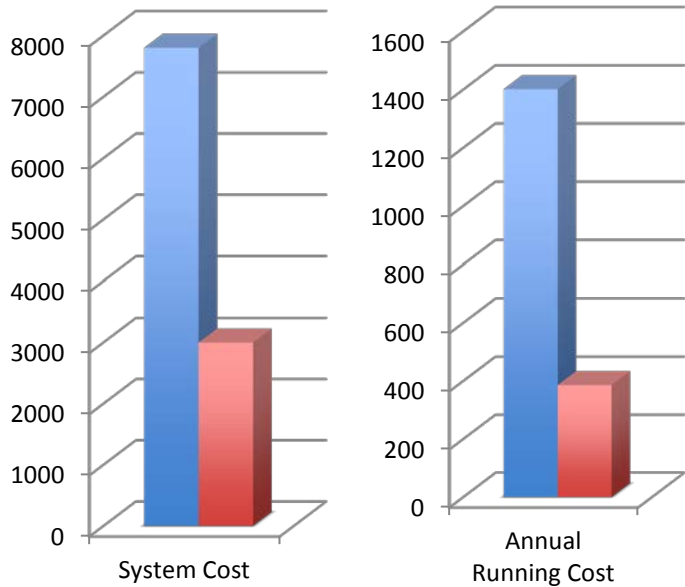


Agoraic Solution



Intel Dual Xeon

# Memcached server cost, power, performance



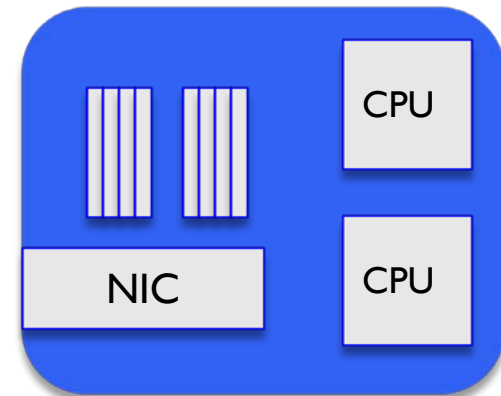
■ Dual Intel Xeon ■ Agoraic

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Annual  
Running Cost

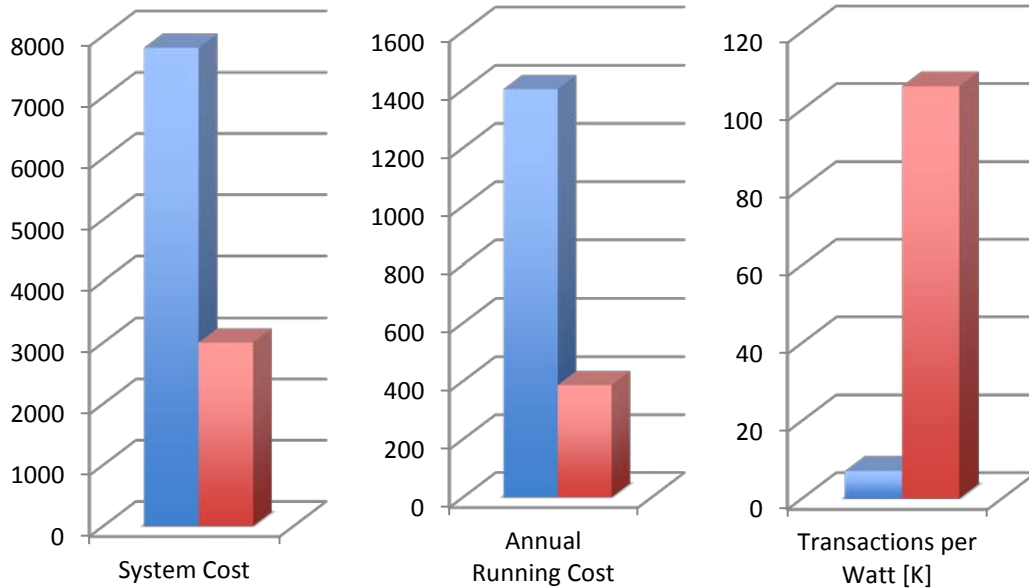


Agoraic Solution



Intel Dual Xeon

# Memcached server cost, power, performance



■ Dual Intel Xeon ■ Agoraic

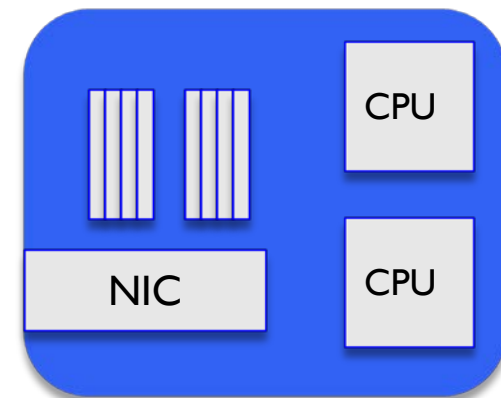
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**15X**  
Transactions  
Per Watt

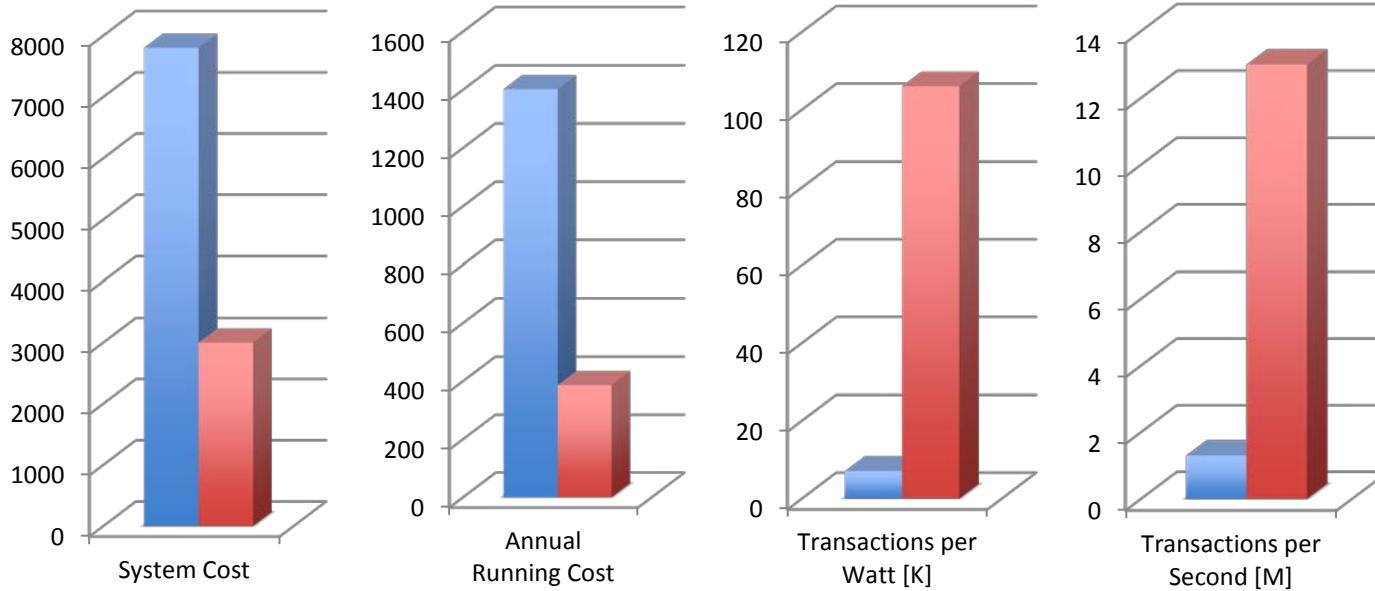


Agoraic Solution



Intel Dual Xeon

# Memcached server cost, power, performance



■ Dual Intel Xeon ■ Agoraic



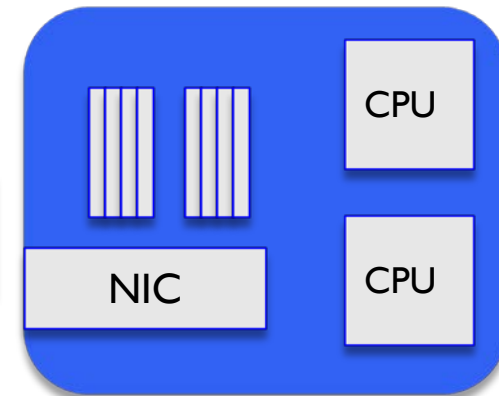
Agoraic Solution

**60% lower**  
System Cost

**73% lower**  
Annual  
Running Cost

**15X**  
Transactions  
Per Watt

**10X**  
Transactions  
Per Second



Intel Dual Xeon

# Scoring Memcached

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## Factors to consider

Volume	Yes, 10-30% of servers 10X server growth by 2020
Low complexity, narrow focus	Yes
Stable design	Yes
Needs lower latency	Yes
Needs better throughput	Yes, but seems achievable with multiple cores as well as HW approach.
Power efficiency matters	Yes, for all objects sizes 90 – 95% power reduction



# Conclusions Memcached HW Acceleration

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## Favorable factors for the FPGA approach

- ▶ 7K queries / Watt vs. 100-200 queries / Watt
- ▶ Significantly better max latency and distribution.

## Some Caveats

- ▶ Similar throughput looks achievable without HW Acceleration
  - Could 64 cores yield 12 million TPS? Need to put this in context with power measurement for TPS per Watt.
- ▶ The FPGA results are experimental vs. the x86 results which included a more comprehensive feature set including exception handling and support for larger numbers of TCP sessions.

# References, links

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- [1] Michaela Blott, Kees Vissers - Xilinx Research, Dataflow Architectures for 10Gbps Line-rate Key-value-Stores  
[http://www.hotchips.org/wp-content/uploads/hc\\_archives/hc25/HC25.50-FPGA-epub/HC25.27.510-Dataflow-Blott-Vissers-Xilinx-final\\_no\\_animation.pdf](http://www.hotchips.org/wp-content/uploads/hc_archives/hc25/HC25.50-FPGA-epub/HC25.27.510-Dataflow-Blott-Vissers-Xilinx-final_no_animation.pdf) and Video: <http://youtu.be/16eoLZ-wIWA>
- [2] ATIKOGLU, B., XU, Y., FRACHTENBERG, E., JIANG, S., AND PALE CZNY, M. Workload analysis of a large-scale key-value store
- [3] WIGGINS, A., AND LANGSTON, J. Enhancing the scalability of memcached. In Intel Software Network (2012).