FPGAs in Flash Controller Applications and More

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Agenda

- FPGAs and Data Centers
- Emerging Memory Types
- Applications I
- Channel I/O Considerations
- Applications II
- Flashing Forward!
Data Center Trends

- **Network Convergence**
  - PCIe in the rack
  - Low latency 10GbE between racks
  - Switch aggregation

- **Algorithmic Acceleration**
  - Big Data
  - Cloud computing applications
    - Financial, Government, Scientific

- **Tiered Storage - Server Caching**
  - Application specific caching
    - Performance (speed and width, latency)
  - Non volatile memory types beyond Flash
FPGA Utilization across Data Centers

Point and SOC Solutions
- Application Acceleration
- Embedded Processing
- I/O Protocol Support
- Memory Control
- Compression
- Security
- Port Aggregation & Provisioning
Application Acceleration
Technology scaling favors programmability and parallelism

Processing Options

- CPUs
- DSPs
- Multi-Cores
- Array
- GPGPUs
- FPGAs

- Single Cores
- Multi-Cores
  - Coarse-Grained CPUs and DSPs
- Coarse-Grained Massively Parallel Processor Arrays
- Fine-Grained Massively Parallel Arrays
Altera FPGA Technology – Hardware Programming

- Massive Parallelism
  - Millions of logic elements
  - Thousands of 20Kb memory blocks
  - Thousands of DSP blocks
  - Dozens of High-speed transceivers

- Hardware-centric
  - VHDL/Verilog
  - Synthesis
  - Place&Route
OpenCL Overview

- Open Computing Language
  - Software-centric
    - C/C++ API for host program
    - OpenCL C (C99-based) for acceleration device
  
- Unified design methodology
  - CPU offload
    - Memory Access
    - Parallelism
    - Vectorization
  
- Developed and published by
  - http://www.khronos.org
OpenCL Process

```c
main() {
    read_data( ... );
    manipulate( ... );
    clEnqueueWriteBuffer( ... );
    clEnqueueNDRange(..., sum,...);
    clEnqueueReadBuffer( ... );
    display_result( ... );
}

__kernel void
sum(__global float *a,
    __global float *b,
    __global float *y)
{
    int gid = get_global_id(0);
    y[gid] = a[gid] + b[gid];
}
```
Multi-Asset Barrier Option Pricing

- Monte-Carlo simulation
  - Heston Model
    \[ dS_t = \mu S_t \, dt + \sqrt{v_t} S_t \, dW_t^S \]
    \[ dv_t = \kappa (\theta - v_t) \, dt + \xi \sqrt{v_t} \, dW_t^v \]
  - ND Range
    - Assets x Paths (64x1000000)

- Advantage FPGA
  - Complex Control Flow

- Results

<table>
<thead>
<tr>
<th>Platform</th>
<th>Power (W)</th>
<th>Performance (Msims/s)</th>
<th>Msims/W</th>
</tr>
</thead>
<tbody>
<tr>
<td>W3690 Xeon Processor</td>
<td>130</td>
<td>32</td>
<td>0.25</td>
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<tr>
<td>nVidia Tesla C2075</td>
<td>225</td>
<td>63</td>
<td>0.28</td>
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<tr>
<td>PCIe385 D5 Accelerator</td>
<td>23</td>
<td>170</td>
<td>7.40</td>
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</table>
TABLE I: Comparison between our OpenCL FPGA and the best CPU implementation of Gzip.

<table>
<thead>
<tr>
<th></th>
<th>Performance</th>
<th>Performance/Watt</th>
<th>Compression Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>OpenCL FPGA</td>
<td>2.71 GB/s</td>
<td>111 MB/J</td>
<td>2.17×</td>
</tr>
<tr>
<td>Intel Gzip</td>
<td>338 MB/s</td>
<td>9.26 MB/J</td>
<td>2.18×</td>
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<tr>
<td>Gap</td>
<td>8.2× faster</td>
<td>12× better</td>
<td>on par</td>
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</table>

Gzip Implementation

- Same compression ratio
- 12X better performance/Watt
Storage Trends
Volatile vs NVM Market Share

Figure 2. Total Memory Revenue Share by Memory Type, Worldwide, 1996-2015

Source: Gartner
Revenue Forecast

Figure 7. Revenue Forecast for Emerging Memory Technologies

Source: Gartner
Flash Cache Challenges & Evolution

- **Ongoing Challenges**
  - Error correction costs increasing
  - Limited endurance (lifetime writes)
  - Slow write speed
  - SATA/SAS SSD interface is slow

- **Storage over PCIe**
  - Faster BW projections
  - SATA Express
  - NVM Express
  - SCSI Express

- **Emerging flash technologies**
  - MRAM (Magneto Resistive)
  - PCM (Phase Change)
  - RRAM (Resistive)
  - NRAM (Carbon Nanotube)
Tiered Storage, Then

Seminole Indian Storage
Tiered Storage, Now

Accelerate Performance
“Time is Money”

- RAM
- FLASH
- Fast HDD
- FAT HDD
- Price
- Power
- Tape & Optical

Consolidate Space Capacity

Reduce Capacity and Data footprint Costs

Balancing Act
Footprint
Cost
Service Level

Source: “The Green and Virtual Data Center” (CRC)

Different Price Bands and Categories

- Enterprise
- Midrange
- SMB
- SOHO

Video/Audio
File Serving
Billing, E-Tail
Database, DSS
Email Messaging
CAD, EDA, SWDev.
Spreadsheets, PPTs, PDFs

Price Bands

Tier-0
Tier-1
Tier-2
Tier-3
Flexibility Required to Support Emerging Memory Technologies

- HDD leveraged as capacity optimized data storage
  - Benefits: Lowest cost per GB/TB for data storage
  - Challenges: Random access, active power & power fail

- NAND SSD leveraged as performance optimized storage
  - Benefits: More IOPS, reduced latency & loss overall power
  - Challenges: Write latency & variability, endurance, power fail

- ST-MRAM leveraged as non-volatile buffer/cache for storage
  - Benefits: DRAM like access, unlimited endurance & power fail
  - Challenges: New storage architecture, density & cost scaling
Hybrid Memory Cube (HMC)

- **HMC technology basics**
  - Ultra high performance, multi-bank DRAM memory
  - DRAM die stacked using state-of-the-art 3D process
  - Built-in memory controller with logic base die

- **Unparalleled gains with HMC**
  - Maximum DRAM bandwidth of up to 160 GB/s
  - Four links running at 15 Gbps offering nearly 1 T bps raw interface bandwidth
  - Up to 4GB density (storage) capacity, low PHY power (pj/bit)
  - Best in class RAS feature set

### Parameters

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Link</td>
<td>4</td>
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<tr>
<td>Speed</td>
<td>10, 12.5, 15 Gbps</td>
</tr>
<tr>
<td>Density</td>
<td>2GB, 4GB</td>
</tr>
<tr>
<td>Vaults</td>
<td>16</td>
</tr>
<tr>
<td>Banks</td>
<td>128, 256</td>
</tr>
<tr>
<td>DRAM B/W</td>
<td>160 GB/s (1.2 Tbps)</td>
</tr>
<tr>
<td>Vault B/W</td>
<td>10 GB/s (80 Gb/s)</td>
</tr>
</tbody>
</table>
Memory Categories

Figure 1. Categories of Memory (Charge Versus Resistivity)

- Memory
  - Electron charge
    - Mass Production: NAND, DRAM, NOR, EEPROM
    - Emerging: Floating Body
  - Resistance
    - Niche: MRAM, FeRAM, Memristor Memory
    - Emerging: PCM, STT-MRAM

Key:
- DRAM = dynamic RAM
- EEPROM = electrically erasable programmable ROM
- EPROM = erasable programmable ROM
- FeRAM = ferroelectric RAM
- MRAM = magnetoresistive RAM
- PRAM = phase-change RAM
- PSRAM = pseudostatic RAM
- SRAM = static RAM

Embedded possible
Figure 2. Comparison of Emerging Memory Technologies

We estimate the comparative capability of these emerging memories in four areas:

- Scalability: Memristor memory > PCM > STT-MRAM
- Read Speed: Memristor memory > STT-MRAM > PCM
- Feature size (cost): STT-MRAM > PCM > Memristor memory

Source: Gartner
## Memory Comparisons - Performance

Table 3. Memory Comparison

<table>
<thead>
<tr>
<th>Feature</th>
<th>SST-MRAM</th>
<th>DRAM</th>
<th>NAND</th>
<th>SRAM</th>
<th>PCM</th>
<th>FRAM</th>
<th>MRAM</th>
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<tbody>
<tr>
<td><strong>Status</strong></td>
<td>Prototype</td>
<td>Product</td>
<td>Product</td>
<td>Product</td>
<td>Product</td>
<td>Product</td>
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<tr>
<td><strong>Cell Element</strong></td>
<td>1T1MTJ</td>
<td>1T1C</td>
<td>1T</td>
<td>6T</td>
<td>1T1R</td>
<td>1T1C</td>
<td>1(2)T1R</td>
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<tr>
<td><strong>Non-Volatile</strong></td>
<td>Yes</td>
<td>No</td>
<td>Yes</td>
<td>No</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
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<tr>
<td><strong>Read Speed</strong></td>
<td>★★★</td>
<td>★★★</td>
<td>★</td>
<td>★★★</td>
<td>★★</td>
<td>★</td>
<td>★★★</td>
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<tr>
<td><strong>Write Speed</strong></td>
<td>★★★</td>
<td>★★★</td>
<td>★★</td>
<td>★★★</td>
<td>★★</td>
<td>★★</td>
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<tr>
<td><strong>Power Consumption</strong></td>
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<td>★</td>
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<td><strong>Endurance</strong></td>
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<tr>
<td><strong>Scalability</strong></td>
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<td>★★★</td>
<td>★★</td>
<td>★★</td>
<td>★★★</td>
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<td><strong>MLC Capability</strong></td>
<td>Yes</td>
<td>No</td>
<td>Yes</td>
<td>No</td>
<td>Yes</td>
<td>No</td>
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<td><strong>New Material</strong></td>
<td>Yes</td>
<td>No</td>
<td>No</td>
<td>No</td>
<td>Yes</td>
<td>No</td>
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<td><strong>Vendors</strong></td>
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<td>Renesas</td>
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<td>TDK</td>
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<td>Samsung</td>
<td>Ramtron</td>
<td>Everspin Technologies</td>
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<td></td>
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<td>Technologies</td>
</tr>
</tbody>
</table>

C = capacitor, FRAM = ferroelectric RAM, MLC = multilevel cell, MRAM = magnetoresistive RAM, MTJ = magnetic tunnel junction, PCM = phase-change memory, R = resistor, SRAM = static RAM, STT-MRAM = spin-transfer torque magnetic random-access memory, T = transistor.

Key: 3 stars = Excellent; 2 stars = Good; 1 star = Reasonable. Red coloring signifies the best in each category.

Source: Gartner
Migration Timeline - Cost

Figure 6. Migration Timeline for Emerging Memory Technologies

Source: Gartner
5MB in Flight!
Convergence.
## Data Center Applications - Servers

<table>
<thead>
<tr>
<th>Application</th>
<th>Usage Examples</th>
</tr>
</thead>
<tbody>
<tr>
<td>Flash SSD</td>
<td>PCIe to ONFI bridging, Flash Control</td>
</tr>
<tr>
<td>Acceleration</td>
<td>Algorithm acceleration for vertical markets</td>
</tr>
<tr>
<td>Bridge Plus</td>
<td>Interface bridging with IP function, e.g. compression and encryption, Dedupe</td>
</tr>
<tr>
<td>I/O Virtualization (10GbE and PCIe)</td>
<td>ASIC alternative; low cost with flexibility</td>
</tr>
<tr>
<td>Co-ASIC</td>
<td>Features enhancement</td>
</tr>
<tr>
<td>Management (BMC, KVM)</td>
<td>IP Flexibility supported with low power</td>
</tr>
</tbody>
</table>
# Data Center Applications - Storage

<table>
<thead>
<tr>
<th>Application</th>
<th>Usage Examples</th>
</tr>
</thead>
<tbody>
<tr>
<td>Flash Cache/SSD</td>
<td>ONFI bridging and RAID adaptor NV DIMM backup, RAID for Flash</td>
</tr>
<tr>
<td></td>
<td><strong>Memory BackUp/Restore</strong></td>
</tr>
<tr>
<td>RAID Bridging</td>
<td>PCIe Gen 3 x8 best of class signal integrity</td>
</tr>
<tr>
<td>Bridge Plus</td>
<td>Interface bridging with IP function</td>
</tr>
<tr>
<td>ASIC Replacement</td>
<td>Lower cost development with flexibility</td>
</tr>
<tr>
<td></td>
<td><strong>Tape</strong></td>
</tr>
</tbody>
</table>
Hybrid RAID System
- Persistent DRAM and Flash Caches

Network Side
- FC HBA
- FC, iSCSI, FCoE

PCI-e or CPU System Bus
- RAID/Cache Controller
- CPU Interface
- CPU
- Network I/F
- RAID² Logic
- Disk I/F
- Cache/Memory Controller

ASSPs

Persistent DRAM

Flash Cache

FPGA Controller

Disk Side
- FC HBA
- SATA
- SAS

Dual Controller
Hybrid RAID System
- PCIe Switch Centric

CPU

Persistent DRAM

PCle Switch

Network Side

PCI-e or CPU System Bus

FC HBA

FC, iSCSI, FCoE

PCI-e

Flash Cache

Dedupe/Encrypt

ASSPs

FPGA Controller

Disk Side

FC HBA

PCI-e

SATA SAS

PCI-e

Dual Controller
Flash Controller Design Considerations
Flash Controller Requirements

- Uncertainty Favors PLDs for Flash Control Solutions
- Flash Challenges Continue
  - Data loss, slow writes, wear leveling, write amplification, RAID
- Many Performance Options
  - Write back cache, queuing, interleaving, striping, over provisioning
- Many Flash Cache Opportunities
  - Server, blade and appliance
Flash Controller Design Challenges

- **Emerging memory types**
  - ONFI 4.0, Toggle Mode 2.x
  - PCM, MRAM
  - DDR4

- **Controller Performance Options**
  - Write back cache, queuing, interleaving, striping

- **ECC levels**
  - BCH, LDPC, Hybrid

- **FTL location** - Host or companion

- **Data transfer interface support**
  - PCI Express, SAS/SATA, FC, IB
Typical SSD Controller Architecture

**Typical Attributes**
- Number of Ports 8 to 32
- Pin Count 250 to 1000+
- Power 1 to 3.5 Watts
- Internal, External RAM

**Variations**
- Number of CPU’s
- Error Correction
- Interfaces
- Memory Type and Size
Mobiveil NVMe SSDC Solution

- DDR3
- NAND
- MRAM

Diagram:
- NVMeFW
- ARM Hard IP
- Altera DDR3 Hard IP
- Interconnect
- Altera PCIe Hard IP
- Avalon MM Bridge*
- NVMe Controller (UNEX)
- PCIe

Interconnect Types:
- On Chip AXI Interconnect
- On Chip APB Interconnect
- Inter block AXI Interconnect
Error Correction Overview

Driving Factors for New ECC
- Increasing Bit errors in NAND Flash
- Soft error occurrences
- Decrease in write cycles
- RS, BCH overhead for data and spare area
- Increase use of Metadata in file systems
- Correction Overhead
- Gate count
- Requirement for no data loss

Comparing ECC Solutions

<table>
<thead>
<tr>
<th>Features</th>
<th>BCH</th>
<th>LDPC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gate Count</td>
<td>High</td>
<td>Mid</td>
</tr>
<tr>
<td>Latency</td>
<td>Low</td>
<td>Medium</td>
</tr>
<tr>
<td>Tuneability</td>
<td>low</td>
<td>high</td>
</tr>
<tr>
<td>Soft Data</td>
<td>no</td>
<td>high</td>
</tr>
<tr>
<td>Data Overhead</td>
<td>high</td>
<td>low</td>
</tr>
</tbody>
</table>

198X       199X       Present
Hamming  RS  BCH

Combined ECC

LDPC
The Parade of Codes

ECC - Block Hamming
- DRAM variant
- Applicable to the flash page block sizes
- Smaller blocks used as error rates increased

Reed Solomon
- CD-ROM basis, stronger than Hamming
- Split correction blocks split into 9 bit symbols
- Good for clumped errors

BCH
- Better supports MLC >8bits correction block
- BCH ECC increasing with correction block sizes
**LDPC and Programmable Logic**

- Addresses higher BER across process node curve
- Good for TLC
- FPGA parallelism of Parity Matrix allows for faster processing of algorithm

![Table showing parity calculations](image)

<table>
<thead>
<tr>
<th>c_1</th>
<th>c_2</th>
<th>c_3</th>
<th>c_4</th>
<th>c_5</th>
<th>c_6</th>
<th>c_7</th>
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<th>c_{10}</th>
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</table>

\[
c_3 \oplus c_6 \oplus c_7 \oplus c_8 = 0
\]
\[
c_1 \oplus c_2 \oplus c_5 \oplus c_{12} = 0
\]
\[
c_4 \oplus c_9 \oplus c_{10} \oplus c_{11} = 0
\]
\[
c_2 \oplus c_6 \oplus c_7 \oplus c_{10} = 0
\]
\[
c_1 \oplus c_3 \oplus c_8 \oplus c_{11} = 0
\]
\[
c_4 \oplus c_5 \oplus c_9 \oplus c_{12} = 0
\]
\[
c_1 \oplus c_4 \oplus c_5 \oplus c_7 = 0
\]
\[
c_6 \oplus c_8 \oplus c_{11} \oplus c_{12} = 0
\]
\[
c_2 \oplus c_3 \oplus c_9 \oplus c_{10} = 0
\]
<table>
<thead>
<tr>
<th>IP</th>
<th>IO</th>
<th>Speed</th>
<th>Logic Density</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>ONFI 3.0</td>
<td>40 pins/ch</td>
<td>400 MTps</td>
<td>5KLE/ch</td>
<td>NAND flash control, wear leveling, garbage collection</td>
</tr>
<tr>
<td>Toggle Mode 2.0</td>
<td>40 pins/ch</td>
<td>400 MTps</td>
<td>5KLE</td>
<td>Same</td>
</tr>
<tr>
<td>DDR3</td>
<td>72 bit</td>
<td>1066 MHz</td>
<td>10KLE</td>
<td>Flash control modes available for NVDIMM</td>
</tr>
<tr>
<td>PCM</td>
<td></td>
<td></td>
<td>5KLE</td>
<td>PCM- Pending production $</td>
</tr>
<tr>
<td>MRAM</td>
<td></td>
<td></td>
<td>5KLE</td>
<td>MRAM- Persistent memory controller (Altera based)</td>
</tr>
<tr>
<td>BCH</td>
<td></td>
<td>&lt;10KLE</td>
<td></td>
<td>Reference design</td>
</tr>
<tr>
<td>PCIe</td>
<td>G3x8</td>
<td>64Gbps</td>
<td>HIP</td>
<td>Flash Cache</td>
</tr>
</tbody>
</table>
**Flash Storage Arrays**

**Target Application:** Enterprise Tier-1 Storage: Databases and Virtualization

<table>
<thead>
<tr>
<th>Function</th>
<th>Solution Rqts</th>
<th>Target Product</th>
<th>IP Rqts</th>
</tr>
</thead>
</table>
| Flash Control   | - ONFI 2.X/3.0  
- Toggle Mode 2.0  
- Multi flash load/ch 
- 40 GPIO/ch      | Arria V        | - Flash Controller  
  (bad block mgt and wear leveling)  
- Metadata & caching  
- ECC BCH core      |
| RAID Control    | PCIe Gen 3                                                                  | Arria 10       | - Flash-specific RAID  
  - Switching and aggregation |
| Power Mgt       |                                                                              | Enpirion       |                                                                        |
**Flash PCIe Cards**

**Target Application:** Embedded PCIe storage for flash cache and scale-out computing

FPGA controller provides flexibility to integrate multiple complex functions and adapt to changing interfaces & APIs.

---

<table>
<thead>
<tr>
<th>Function</th>
<th>Solution Rqts</th>
<th>Target Product</th>
<th>IP Rqts</th>
</tr>
</thead>
<tbody>
<tr>
<td>Flash Control</td>
<td>- ONFI 2.X/3.0&lt;br&gt;- Toggle Mode 2.0&lt;br&gt;- Multi flash load/ch&lt;br&gt;- 40 GPIO/ch&lt;br&gt;- PCIe Gen 3 x8&lt;br&gt;- Low power &amp; cooling</td>
<td>Arria V</td>
<td>- Flash Controller (bad block mgt and wear leveling)&lt;br&gt;- Flash RAID&lt;br&gt;- Cache controller&lt;br&gt;- BCH core&lt;br&gt;- PCIe config &lt; 100msec&lt;br&gt;- Host interface/APIs</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Arria 10</td>
<td></td>
</tr>
</tbody>
</table>

---

PCIe: Gen 3x8
Flash Cache Controller Examples

- **Multi Channel Controller**
  - Single to multi Flash channel capability
  - Basic NAND development platform
  - Provides High Speed ONFI & Toggle NAND PHY
  - ECC of 8 and 15 bits of error correction

- **Single Channel Controller**
PCle to RAID controller

Embedded storage for flash cache and high performance computing

<table>
<thead>
<tr>
<th>Function</th>
<th>Solution Rqts</th>
<th>Target Product</th>
<th>IP Rqts</th>
<th>IP Partner</th>
</tr>
</thead>
<tbody>
<tr>
<td>RAID Control</td>
<td>- ONFI 2.X/3.0</td>
<td>Arria 10</td>
<td>Flash Controller RAID</td>
<td>SLS CAST</td>
</tr>
<tr>
<td></td>
<td>- Toggle Mode 2.0</td>
<td></td>
<td>PCIe config &lt; 100msec</td>
<td>Altera Reference Design (3Q12)</td>
</tr>
<tr>
<td></td>
<td>- Multi flash load/ch</td>
<td></td>
<td>6Gb SAS/SATA</td>
<td>CEVA/Inteliprop</td>
</tr>
<tr>
<td></td>
<td>- 40 GPIO/ch</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>- PCIe Gen 3</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>- 6Gb SAS/SATA</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

SSD Interface (SAS/SATA)
Memory Lookup and Cache

Target Application

Embedded Memory search and cache for high performance computing

<table>
<thead>
<tr>
<th>Function</th>
<th>Solution Rqts</th>
<th>Target Product</th>
<th>IP Rqts</th>
<th>IP Partner</th>
</tr>
</thead>
</table>
| Memory Control | -ONFI 2.X/3.0  
-Toggle Mode 2.0  
-Multi flash load/ch  
-40 GPIO/ch  
-PCIe Gen 2 x8/Gen3 x8  
-Interlaken | Arria V  
Arria 10 | Flash Controller  
PCIe config < 100msec  
6Gb SAS/SATA  
“Look-aside variant” | SLS CAST |
Development Platforms

- Stratrix/Arria FPGA
- Everspin 64MB DIMM
- Introspect I/O Tester
- Gidel ProceV Board
- Micron Daughter Card
- Cyclone Development Board
System IO Considerations
System IO

- System Application Requirements
  - Performance- bandwidth
  - IO network
  - Memory
  - Latency
Hardened IP (HIP) Advantages

- Resource savings of 8K to 30K logic elements (LEs) per hard IP instance, depending on the initial core configuration mode
- Embedded memory buffers included in the hard IP
- Pre-verified, protocol-compliant complex IP
- Shorter design and compile times with timing closed block
- Substantial power savings relative to a soft IP core with equivalent functionality
PCI Express NVMe

- Scalable host controller interface for PCIe-based solid state drives
- Optimized command issue and completion path
- Benefits
  - Software driver standardization
  - Direct access to flash
  - Higher IOPS and MB/s
  - Lower latency
  - Reduced Power Consumption
Intel QPI

- Up to (2) full width QPI 1.1
  - 6.4, 8.0 Gbps
- Designed for QPI Electricals
  - Common Mode Voltage
  - Lane detection on die
- Chip to chip interconnectivity
- Fast HP 28nm. process
- Hard PHY + Upper Layers Option
  - Decrease latency, power, & fpga logic
  - Use “Embedded Hardcopy Blocks”
  - Improve throughput by 75+%  
    - 6-8GB/s data payload each way

Note: Routing Layer not used
Industry Interface Convergence

**Enterprise**
- 2012: SATA 6Gb, SAS 6Gb, PCIe 4-8Gb (SATA)
- 2013: ONFi 2,3, Toggle 1,2
- 2014: ONFi 2, 3, 4, Toggle 2, Joint Spec Devices
- 2015: ONFi 2, 3, 4, Joint Spec
- 2016: ONFi 2, 3, 4, Toggle 2, Joint Spec Devices
- 2017: ONFi 2, 3, 4

**Ultra Mobile/Desktop**
- 2012: SATA 6Gb, PCIe 4/8 Gb SATA
- 2013: SSD (ONFI 2), Cache (ONFI 2, Toggle)
- 2014: ONFI 2, 3, 4, Joint Spec
- 2015: ONFI 2, 3, 4, JS
- 2016: ONFI 2, 3, 4, Joint Spec
- 2017: ONFI 2, 3, 4

**Tablet**
- 2012: eMMC 4.4, MIPI
- 2013: eMMC 4.6, UFS, PCIe, PCIe mobile
- 2014: eMMC 4.6, UFS
- 2015: eMMC 4.6, ONFI 2, 3, 4 JS
- 2016: eMMC 4.6, MIPI, UHS2, PCIe, PCIe mobile
- 2017: eMMC 4.6, MIPI, UHS2

**Smartphones**
- 2012: eMMC 4.1, Raw NAND SLC/MLC, DDR NVM
- 2013: eMMC 4.1, Joint Spec
- 2014: eMMC 4.1, Joint Spec
- 2015: eMMC 4.1, Joint Spec
- 2016: eMMC 4.1, Joint Spec
- 2017: eMMC 4.1, Joint Spec
- Flash Controllers manage SAS/SATA SSD interfaces
- 12Gbps SAS support required for enterprise drives
- FPGA transceivers need to support electrical performance and OOB signaling
6G SAS Demo

SAS Cable Connection to SAS peer (via connector mezzanine board)

SAS peer is Lecroy SAS Sierra M6-2 or various SAS HDD

PC running SSD Emulation Windows Driver or CEVA SASTool test software (as if embedded processor)
FPGA Flash Applications - Part Two
DRAM Cache Backup

- Data Center server power outages continue
- Read/Write Consequences
  - Data Loss
  - Undetected errors in host application
- NVDIMM designs protect system integrity but...

<table>
<thead>
<tr>
<th>Battery Limitations</th>
<th>Issue</th>
</tr>
</thead>
<tbody>
<tr>
<td>Shelf Life</td>
<td>One year max or 500 cycles</td>
</tr>
<tr>
<td>Disposal and Handling</td>
<td>Hazardous Waste Management</td>
</tr>
<tr>
<td>Data Storage Capacity</td>
<td>Up to 72 hours</td>
</tr>
<tr>
<td>Down Time</td>
<td>Charge Time up to 6 hours</td>
</tr>
<tr>
<td>Replacement Cost</td>
<td>Field Time and Materials</td>
</tr>
</tbody>
</table>
The Perfect Storm

- Technology Enablers
  - **Super Capacitors** are production worthy
  - **Flash memory** costs continue to decline
  - **FPGA** technology meeting power/performance/cost

![Image of NAND Flash Accelerates Moore's Law graph]

- **NAND Flash Accelerates Moore's Law**
- Intel Micron, Samsung, Toshiba/Sandisk, Hynix/ST

![Image of FPGA power consumption diagram]

- FPGA Low Power Attributes
- **30% Lower** Core Power (W) vs Logic Elements (K)
Memory Backup

Target Application
Nonvolatile DIMM for data recovery backup and restore

Benefits vs Batteries

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Ultracapacitors</th>
<th>Batteries</th>
</tr>
</thead>
<tbody>
<tr>
<td>Environmental</td>
<td>Green</td>
<td>Hazardous disposal</td>
</tr>
<tr>
<td>Shelf Life</td>
<td>Years</td>
<td>Months</td>
</tr>
<tr>
<td>Charge Time</td>
<td>Seconds</td>
<td>Hours</td>
</tr>
<tr>
<td>Conditioning</td>
<td>None</td>
<td>Initial and periodic</td>
</tr>
<tr>
<td>Weight</td>
<td>Lighter</td>
<td>Heavier</td>
</tr>
<tr>
<td>Operating Temp</td>
<td>Up to 70°C</td>
<td>60°C max</td>
</tr>
<tr>
<td>Operating Life</td>
<td>Up to 10 years</td>
<td>1 to 3 years</td>
</tr>
<tr>
<td>Maintenance</td>
<td>None</td>
<td>Replace very 1-2 years</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Component/Circuit</th>
<th>Function</th>
<th>Component Benefit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cyclone V FPGA</td>
<td>Circuit management and control</td>
<td>Low power (28nm), DDR3 memory, and ONFI Flash control</td>
</tr>
<tr>
<td>High Speed Switching FETs</td>
<td>DDR3 Switch Signaling</td>
<td>Switching with noise suppression</td>
</tr>
<tr>
<td>ONFI NAND Flash</td>
<td>Memory Cache</td>
<td>2-8GB, matches DRAM density</td>
</tr>
<tr>
<td>DDR3 DRAM</td>
<td>Memory Source</td>
<td>2-8GB</td>
</tr>
<tr>
<td>Charging Circuit</td>
<td>Low Power, Green Energy Supply</td>
<td>Ultra Capacitor Bank with optional battery supply</td>
</tr>
<tr>
<td>Processor</td>
<td>Power Good Signal</td>
<td>Circuit toggle</td>
</tr>
</tbody>
</table>
NVDIMM Controller Architecture

- Processor
- DDR
- FPGA (Cyclone)
- DIMM

On power failure, these FETs switch out the processor signals.

Can be:
- Buffered
- Un-buffered
- Registered

- 400MHz / 800MB tested
- Power failure switch
- Individual CKE lines
- DDR ctrl with tri-state
- I2C

Control signals

To super-cap bank

- Power regulation
- Flash 1 or 2 SD Cards or BGA

5 or 9

Can be:
- Buffered
- Un-buffered
- Registered
Nanosecond-class MRAM Storage

500x Performance...

<table>
<thead>
<tr>
<th></th>
<th>NAND</th>
<th>MRAM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Density</td>
<td>64Gb</td>
<td>1Gb</td>
</tr>
<tr>
<td>Latency</td>
<td>50us</td>
<td>45ns</td>
</tr>
<tr>
<td>4k Write IOPS</td>
<td>800</td>
<td>400k</td>
</tr>
<tr>
<td>Cost/GB</td>
<td>1</td>
<td>50</td>
</tr>
</tbody>
</table>

...at only 50x Cost/GB
FPGA Benefits Summary

- High System Performance
- Design Flexibility
- Memory Bandwidth
- Signal Integrity
- Low Power
- Embedded Processing
FPGAs are a great technology option for Data Centers
- Networking: Port aggregation
- Compute: Application Acceleration
- Storage: Controllers for non volatile memories

All development phases supported
- Prototyping
- Production
- Test Validation
- Upgrades
Innovation Leader Across the Board

CPLDs
Lowest Cost, Lowest Power

FPGAs
Cost/Power Balance
SoC & Transceivers

FPGAs
Mid-range FPGAs
SoC & Transceivers

FPGAs
Optimized for
High Bandwidth

PowerSoCs
High-efficiency
Power Management

Embedded Soft and Hard Processors

Design Software

Development Kits

Intellectual Property (IP)
- Industrial
- Computing
- Enterprise