eLDPC Codes

Designing Error Floor Performance of Iterative Codes

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General LDPC Code Construction

- Good LDPC code construction addresses three areas of performance:
  - Water fall performance
  - Error floor performance
  - Minimum distance (Misscorrection performance)

- Performance in all three areas is achieved by careful choice of LDPC code internal structure.

- The aspects of the LDPC code performance have opposite requirements on the internal structure of the code.

LDPC Codes for SSD’s

- The LDPC codes for SSD’s have additional requirements:
  - High code rate R>0.9
  - High throughput
  - Extremely low error floor performance SFR<1e-13 (UBER<1e-16)
- Trade-off between throughput, internal structure and error floor performance is becoming increasingly hard.
- Verifying the error floor performance of the LDPC codes is becoming unfeasible.
- Verifying SFR=1e-13 takes 3 years on FPGA board with 1GB/s LDPC throughput.
  - 10 error occurrences

Traditional Approaches to Error Floor Mitigation

- Outer BCH code to remove the error floor
  - Code rate penalty ~2% for T=10 and 1KB
  - Additional area and power
- Post processing
  - Reliable mapping of trapping sets
  - Additional memory and latency
- High density parity matrix
  - Throughput impact (~25% lower throughput cw=5 vs. cw=4)
  - Possibly hard or impossible to construct given the constraints (QC, rate)
- RAID
  - Significant additional parity required
  - Latency and throughput penalties

eLDPC Codes

- The eLDPC codes are the new class of the LDPC-like codes addressing the error floor performance:
  - No additional HW resources
  - No throughput penalty
  - Error floor performance guaranteed by construction
  - Error floor performance verifiable in a day

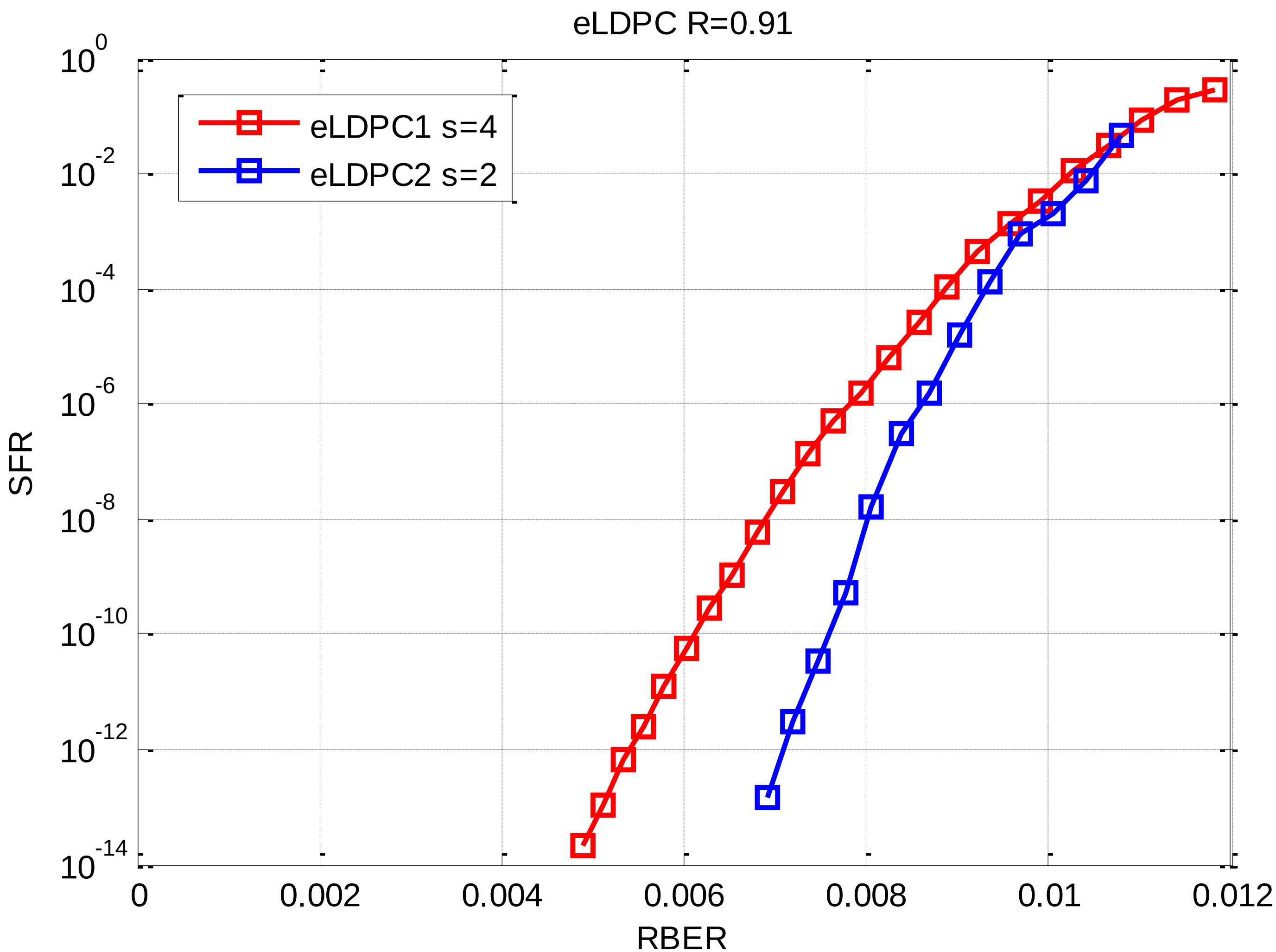
eLDPC Code Structure

- In addition to raw and column degree distribution new design parameter, spreading factor S
- The code rate of the eLDPC code:

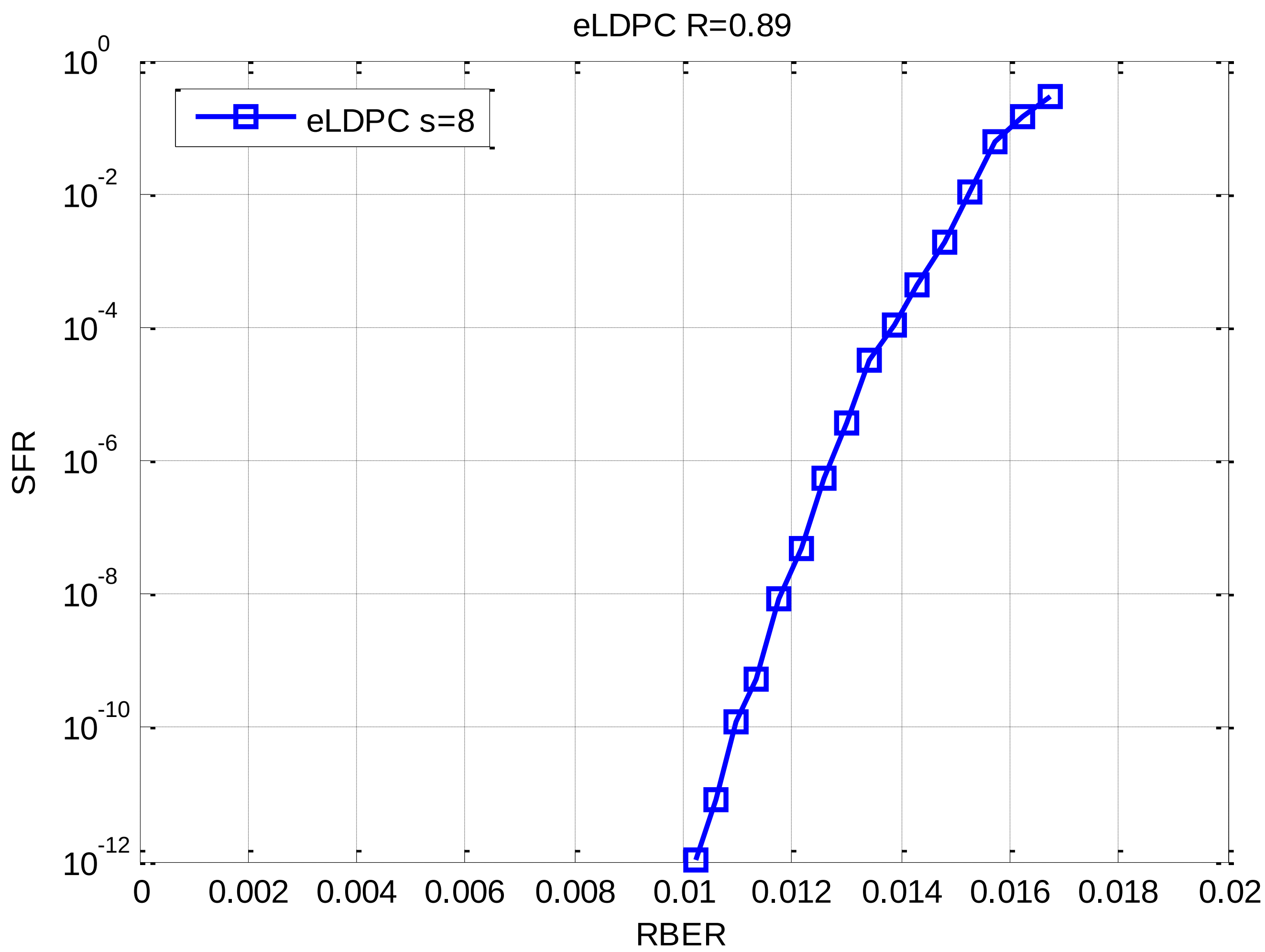
$$r = \frac{s\left(1 - \frac{\int_0^1 \rho(x)}{\int_0^1 \lambda(x)}\right)}{s + \frac{\int_0^1 \rho(x)}{\int_0^1 \lambda(x)}}$$

- The performance upper bound based on the importance sampling measurement.

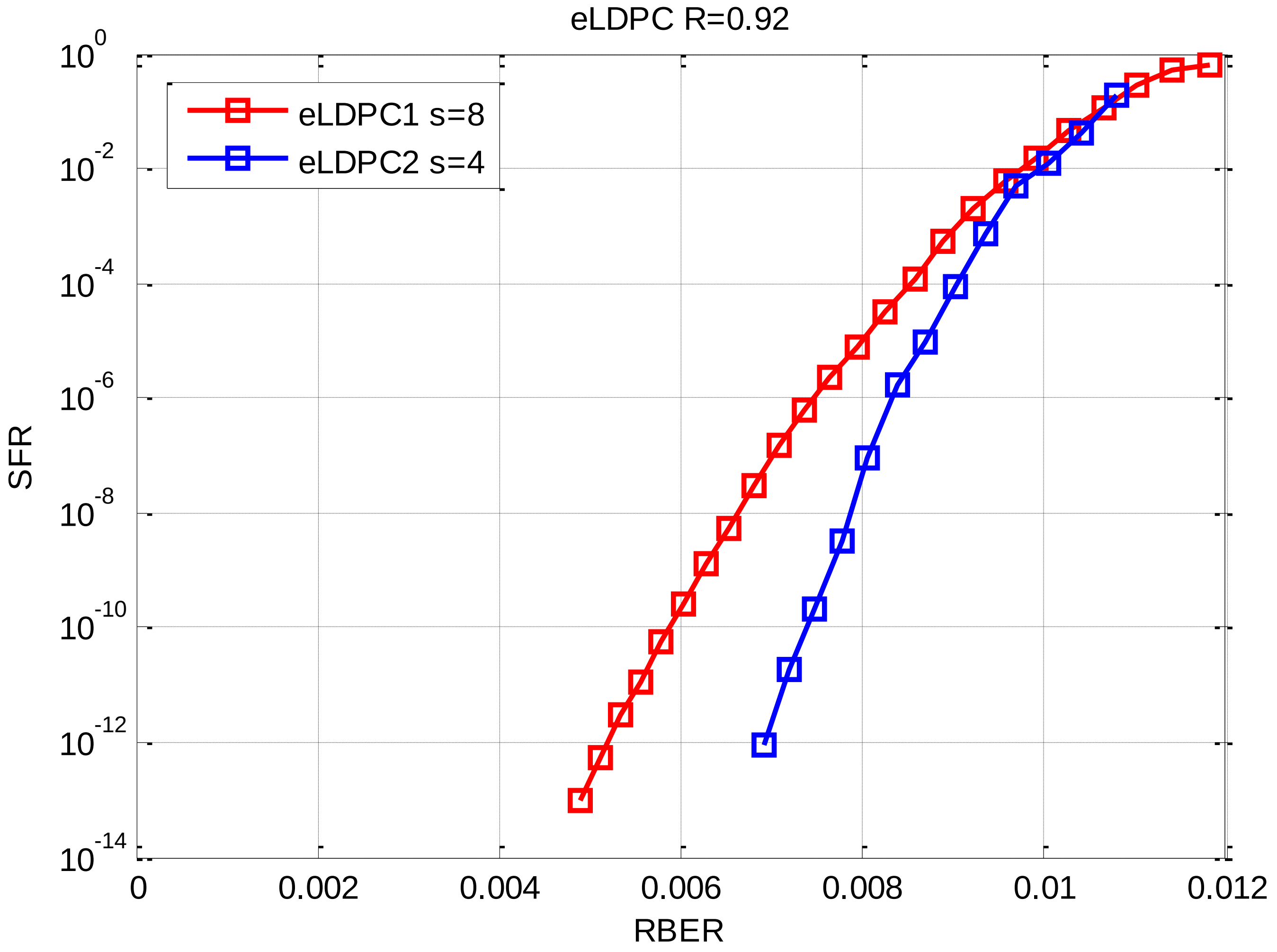
eLDPC 2KB R=0.91



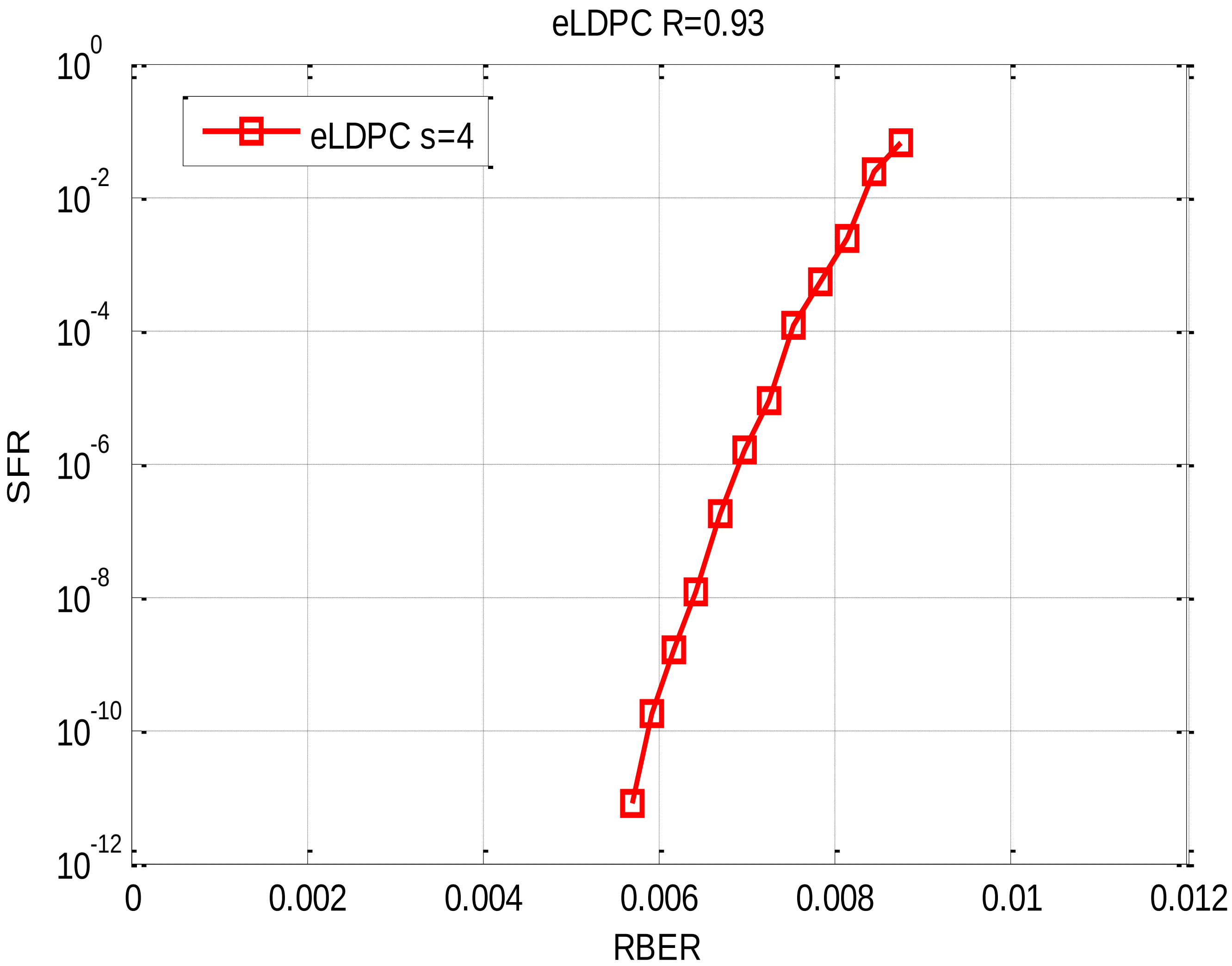
eLDPC 4KB R=0.89



eLDPC 4KB R=0.92



eLDPC 2KB R=0.93



Conclusion

- eLDPC codes have deterministic error floor behavior
- eLDPC codes enable fast application deployment
  - Short code construction phase
  - Short performance verification phase
- eLDPC codes provide higher throughput