Overcoming the Challenges of 10nm-class NAND Flash Memory

Yan Li, Ph.D
Sr. Director of NAND Design
SanDisk Corporation
During our meeting today we will be making forward-looking statements.

Any statement that refers to expectations, projections or other characterizations of future events or circumstances is a forward-looking statement, including those relating to market demand, market growth, industry trends, expenses, future memory technology, and technology transitions and future products.

Actual results may differ materially from those expressed in these forward-looking statements due to the factors detailed under the caption “Risk Factors” and elsewhere in the documents we file from time-to-time with the SEC, including our annual and quarterly reports.

We undertake no obligation to update these forward-looking statements, which speak only as of the date hereof.
Outline

❖ Demand for Flash Memory

❖ Challenges and Developments in 10-nm Class NAND

❖ Future Development

❖ Final Notes
Demand for NAND Flash Memory
NAND Flash Bit Forecast (billions of GB)

- Gartner Jun-13 - supply
- FI Jun-13 - demand
- iSuppli Jun-13 - shipment
- DRAMeX Jun-13 - demand
- Average
NAND vs. DRAM Cost Delta: New Opportunities

NAND: 10X cost advantage

Cost ($/GB)

Source: Gartner Forecast
Flash Memory Summit 2013
Santa Clara, CA

- Slower NAND scaling due to more complex process and fundamental changes in lithography
- Electrical/physical limits of NAND, higher density, and $/GB scaling will require 3D approaches
SanDisk Technology Strategy

2D NAND
- Efficient and Scalable 3D NAND Architecture
- Easy system adoption due to similarity to 2D NAND

3D BiCS
- Bit Cost Scalable NAND

3D ReRAM
- 32 Gb Test Chip Successfully Made on 24nm node
- Potential to Scale Below 10nm
Challenges and Developments in 10-nm Class NAND
The Effect of Scale Down (Technology Shrink)

Vt distributions wider because of less control over the cell uniformity and small amount electrons in FG.
3 bits per cell continue in 1Ynm and 1Znm
More applications will use 3 bits per cell for cost reduction
Cycling and data retention result in shift and widening of the Vt distribution.

VT Shift after Data Retention

Low cycling counts

Higher Cycling counts

Cycling

Data Retention
Factors Affecting Flash Memory P/E cycle

- Limited endurance in Flash Memory is due to Tunnel-Oxide Degradation and trap generation
- Thinner Oxide can help → less data retention
- Heating to get the traps out?
The Effect of Cell to Cell Interferences

Interferences and noise cause the Vt Distribution to shift and widen.
Overcome Cell to Cell Coupling – WL Order

**Step 1:** 2 states Program

When (1) is programmed

D

V_{Low1}

**Step 2:** Coarse Program

When (4) is programmed

G

V_{Low2}

**Step 3:** Fine Prog

When (8) is programmed

G

V_{Tar}

RCCC
P/E Cycle/Data Retention/Performance Tradeoff

For the same DR margin, reduction in DR time can be traded in for higher endurance.

Smaller program voltage step size: narrower distributions (for more DR/cycling margin) but longer programming time.

Less ECC

More ECC

Cycle

ECC (or tPROG)

Trade Off

DR

Less Cycles

More Cycles

HTDR Vt Shift

DR margin

Log (Bake Time)

Log (Cells)

Δ Vt

Vt

Smaller Prog Step Sizes
Energy Reduction – Lower Supply Voltage

- Power Supply get lower for energy reduction

VCCQ = 3.3V (from Host)

- Voltage regulator

VCC = 3.3V (from Host)

- Voltage regulator

- VCCQ = 1.8V (from Host)
  - ~50%
  - ~30%

- VCC = 1.8V (from Host)

- 2.5V

- 1.6V

- Logic Peripheral Block
- Data-Path Block
- Page Buffer
- Low Voltage Analog
- High Voltage Analog

Small Swing

Flash Memory Summit 2013
Santa Clara, CA
Energy Reduction – External Pump Supply

- High Voltage generation may cost more power with lower VCC supply
- External pump device could be more efficient

VCCQ=1.8V (from Host)

VCC=1.8V (from Host)

VPP=12V-24V (pump chip)

The JEDEC standard NAND Flash Interface 0.62. VPP=12V
High Speed IO Interface Toggle Mod

- CE#
- ALE
- CLE
- RE#
- WE#
- R/B#
- WP#
- I/O[7:0]

NAND Toggle Mode

Controller

- CE#
- ALE
- CLE
- RE#
- WE#
- R/B#
- WP#
- I/O[7:0]

<table>
<thead>
<tr>
<th>Interface Speed</th>
<th>All NAND</th>
<th>2xnm</th>
<th>1x-1ynm</th>
<th>1znm</th>
<th>3D NAND</th>
</tr>
</thead>
<tbody>
<tr>
<td>50MB/s</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>200MB/s</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>400MB/s</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>533MB/s</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>800MB/s</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- Interface Speed impact on System performance
- 800MB/s need new transistors (extra process cost)
Future Development
3D NAND Technology
BiCS
- Doesn’t require EUV
- Regular optical tools for less stringent HP
- Large cell for better reliability

Yield Challenge
- High aspect Ratio
- Multiple stack patterning
- Defect in 3-D structure

BiCS offers Cost cutting and overcome 2-D NAND scaling issues
3D ReRAM

- SanDisk R&D making steady progress in 3D ReRAM
- 3D ReRAM R&D Paper Presented at ISSCC 2013

3D ReRAM may scale to below 10nm node
Final Notes

Overcome the Challenges of 10nm–class NAND Flash

- Advanced system management
  - Intelligent memory managements and algorithm
  - Trade off performance, data retention and endurance
- Enhanced system performance
  - High speed IO interface
  - Reduced energy consumption to allow massive parallel operations
- Advanced New Technologies on the Horizon
  - 3D NAND & ReRAM

The Flash industry needs breakthroughs to take advantage of the explosive storage demand in the digital age

Flash Memory continues to be the storage king