Design Considerations for UFS & eMMC Controllers

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Agenda

- Mobile Storage in SoC
- Challenges in Mobile Storage Controller Designs
- Enabling Mobile Storage Design Ecosystem
- Summary
Multiple Mobile Storage Interfaces in Application Processor

**Video**
- Touch Screen
- Audio Spkr, Mic Hdset
- LCD Display
- Camera
- 4G/3G Modem
- Wi-Fi

**Audio & Display**
- MIPI CSI-3
- MIPI DSI
- Display
- Slimbus
- MIPI DSI
- HDSET
- Speaker, Mic
- HDMI 1.4a

**Aps Processors**
- GPMC
- SDIO
- UART
- GPIO
- IrDA
- Keyboard
- System Clock
- 3DTV Controller
- PC
- CLK

**Bus Controllers**
- LPDDR2 DRAM
- SD 3.0/4.0
- UFS 1.1 / 2.x
- eMMC 4.51 / 5.x

**Typical Mobile Application Processor**
- SDIO
- USB2.0/3.0 OTG
- USB3.0 OTG
- SATA-2
- SSD
- USB Device
- Flash

- Compliance
- Backward Compatibility
- Interoperability
Mobile Storage Evolution Faster Than Ever

UFS

SD

eMMC

Challenges of Backward Compatibility eMMC

<table>
<thead>
<tr>
<th></th>
<th>eMMC 4.41</th>
<th>eMMC 4.51</th>
<th>eMMC 5.0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Max Throughput</td>
<td>High Speed 832 Mbps</td>
<td>HS200 1.6 Gbps</td>
<td>HS400 3.2 Gbps</td>
</tr>
<tr>
<td>Data Lines</td>
<td>4 or 8-bit</td>
<td></td>
<td>8-bit</td>
</tr>
<tr>
<td>Signal Count</td>
<td>10 Pins</td>
<td></td>
<td>11 Pins (Data Strobe)</td>
</tr>
<tr>
<td>IO Voltages</td>
<td>1.2 V / 1.8 V</td>
<td>1.2 V / 1.8 V</td>
<td></td>
</tr>
<tr>
<td>Interface</td>
<td>DDR-52</td>
<td>HS200</td>
<td>HS400</td>
</tr>
<tr>
<td>Data Strobe</td>
<td>No</td>
<td></td>
<td>Yes</td>
</tr>
<tr>
<td>Tuning (Read)</td>
<td>No</td>
<td></td>
<td>Yes</td>
</tr>
<tr>
<td>Clock (MHz)</td>
<td>0 – 52 MHz</td>
<td></td>
<td>0 – 200 MHz</td>
</tr>
</tbody>
</table>
eMMC Compliance

- eMMC Device spec published by JEDEC
- Compliance can be done through 3rd party Compliance Testers
  - No formal compliance guidelines
## Challenges of Backward Compatibility UFS

<table>
<thead>
<tr>
<th></th>
<th>UFS 1.0</th>
<th>UFS 1.1</th>
<th>UFS 2.0</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Transaction Layer</strong></td>
<td>Host Interface</td>
<td>HCI 1.0</td>
<td>HCI 1.1</td>
</tr>
<tr>
<td><strong>Link Layer</strong></td>
<td>UniPro™</td>
<td>v1.40</td>
<td>v1.41</td>
</tr>
<tr>
<td># of Lanes</td>
<td>Single Lane</td>
<td>Single Lane</td>
<td>2-Lane</td>
</tr>
<tr>
<td><strong>Physical Layer</strong></td>
<td>M-PHY</td>
<td>v1.0</td>
<td>v2.0</td>
</tr>
<tr>
<td>Data Rate</td>
<td>1.5 Gbps</td>
<td>2.9 Gbps</td>
<td>5.8 Gbps</td>
</tr>
<tr>
<td># of Lanes</td>
<td>1</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td>Interface</td>
<td>Tx +/-, Rx +/-</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Diff V&lt;sub&gt;peak-peak&lt;/sub&gt;</strong></td>
<td>500 mV Max (non-terminated)</td>
<td>250 mV Max (terminated)</td>
<td></td>
</tr>
</tbody>
</table>

Source: JEDEC
## UFS 1.1 Compliance

<table>
<thead>
<tr>
<th>Layer</th>
<th>Protocol</th>
<th>Rev.</th>
<th>Test Spec</th>
<th>Certification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transaction</td>
<td>UFS</td>
<td>1.1</td>
<td>UFS Test Spec v1.0</td>
<td>UFSA</td>
</tr>
<tr>
<td>Link Layer</td>
<td>UniPro</td>
<td>1.41</td>
<td>UniPro CTS_v1.0_r01</td>
<td>MIPI / UNH-iOL</td>
</tr>
<tr>
<td>PHY Layer</td>
<td>M-PHY</td>
<td>2.0</td>
<td>M-PHY CTS_v0.99</td>
<td></td>
</tr>
</tbody>
</table>
Design Challenges

1. Compliance to Industry Standard(s)
   - JEDEC
   - MIPI® Alliance
   - eMMC UFS
   - UniProSM M-PHY®
   - Physical Layer
   - Link Layer
   - Application Layer
   - SDA
   - SD SDIO
   - UFSA

2. Backward Compatibility
   - eMMC 4.3 → 4.4 → 4.5 → 4.51 → 5.x
   - UFS 1.0 → 1.1 → 2.x
   - UniPro 1.40 → 1.41 → 1.6x
   - M-PHY 1.0 → 2.0 → 3.x
   - SD 2.0 → 3.0 → 4.0 → 4.x
   - UHS-II → UHS-?

3. Inter-Operability
   - Data/File Transfer
   - Read/Write Commands
   - Link Initialization

Can I have all these validated before starting my SoC design?
M-PHY® Verification
Before Silicon
M-PHY Verification
Before Silicon

- Reset & Initialization
- Scoreboarding
- Coverage Collection
- Constrained random stimulus
- Functional Check
M-PHY Verification Cases

- HW Reset test
- Attribute read/write test
- HS/LS Modes and Power
- State Re-configuration Test
- Error Injection Test
- Timing – Gate Level Simulation

M-PHY Verification Cases Diagram:

1. **Sequencer** → **M-PHY Agent** → **Coverage** → **Scoreboard** → **M-PHY Agent** → **Coverage** → **Sequencer**
2. **UVC RMMI Master** → **VIP** → **UVC RMMI Monitor** → **CTRL** → **DUT M-PHY** → **DPDN** → **UVD DPDN Monitor** → **VIP** → **UVC DPDN**
UFS Controller Verification
Before Silicon (UFS-HCI + UniPro)
Migrate to FPGA based System

- A black-box approach enables quick access to a validation platform
- FPGA with Verified UFS IP
FPGA System for Device Validation & Software Development

Host

Device

Certified UniPro

Verified and Tested UFS-HCI or System Bus Interface

Verified and Tested Driver and Stacks

Tested M-PHY Signals
Enabling UFS/eMMC Design Ecosystem

- FPGA based Development Platform productized into Validation Platform
  - IP, software stacks and PHY come together
- Used **by IP vendor** (e.g., Arasan) for Interoperability testing with other pioneers
- Used **by Test & Measurement vendors** as target platforms
  - For validation of protocol generators and analyzers
- Ultimately used **by SoC/Device vendors** as target or reference platforms for silicon validation
  - Assured of IP interoperability, compliance, and backward compatibility
Summary

- New JEDEC storage standards continue to evolve for new markets
  - Early IP/SoC validation enables compliance and compatibility for fast time-to-market

- Different SoC vendors at different stages of spec adoption
  - Different spec revisions from different OEM’s
  - Backward compatibility and Interoperability a must among vendors

- IP vendors continue to
  - Lead the pack in transforming specs to RTL and GDSII
  - Keeping backward compatibility with older standards in new designs
  - Enabling ecosystem-wide Inter-Op and compliance through
    - Software stacks
    - Hardware Validation Platforms

All items available before starting your SoC/Device designs!!
THANK YOU