Intelligent Embedded Systems

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The Times, They are a Changing...
Evolving Embedded Systems
The Integration of Intelligence

Apps / Integration

Specialized Function

Endpoint / Sensor

Source: IDC

25 billion devices by 2020
Don’t just take my word for it...

UBM 2012 Embedded Market Survey – May’12

Does your current embedded design have...?

Networking 58%
Wireless 38%
Graphical UI 40%
Touch Screen 16%

~100 %

* Angry Bird results estimated
Embedded World and Mobile/Compute World Collide

- **Compute World**
  - Mobility
  - Flexibility
  - Rapid Innovation

- **Embedded World**
  - Stability
  - Longevity
  - Quality/Reliability
Embedded World and Mobile/Compute World Collide

**Compute World**
- Open Connectivity
- Standard OS/Cores
- User accessible

**Embedded World**
- No / Proprietary connectivity
- Custom OS/CPU
- Closed Systems
Creation of Intelligent Systems Segment

Billions of Systems

- $649B today
- $1.4T by 2016

Traditional Embedded

Intelligent Systems

Multi-core/Advanced Processors
Always on/intelligent connectivity
High-level OS & User-Machine I/F
Data Generation & Analysis

Source: IDC
Security & Other Implications

- Standardized operating systems and building block components becoming more prevalent in non-PC architectures
- Always-on connection provides another conduit for infection
- Advanced Persistent Threats difficult to detect and damaging to embedded systems

Source: McAfee Threats Report Q1-2012
Protection starts at boot

- Tamper-proof firmware in BIOS or boot loader using locking or other cryptographic security measures for NOR flash memory
- Measurement and attestation of image to confirm root of trust
  - Leverage techniques available with Trusted Computing and a Trusted Platform Module, if available
- Additional security primitives from NOR flash memory are available
  - Code/data integrity, binding to the system though cryptographic means
  - Last line of defense against physical tampering of the system
 Complexity, code size, and latency

High-level OS, UIs and connectivity in Intelligent systems are driving code size growth

At larger sizes, simple SPI NOR has growing performance considerations
Full Chip Read Time

- 133Mhz x16 Sync
- 52Mhz x16 Sync
- x16 Page Mode
- 108MHz x4 SPI
- 108MHz x8 SPI

Full chip Read Time (seconds)

128Mb  256Mb  512Mb  1Gb  2Gb
**Bandwidth Efficiency**

- **I/O Transfer Rate (MB/s)**
  - 133MHz x16 AAD Sync
  - 52Mhz x16 Sync
  - x16 Page Mode
  - 108MHz x8 SPI
  - 108MHz x4 SPI
  - 50MHz x1 SPI

* Bubble size shows BW/pin

**Signal Pin Count**

- 0
- 10
- 20
- 30
- 40
- 50
- 60

**Bandwidth Efficiency**

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Future Serial Interface

Bandwidth Efficiency

I/O Transfer Rate (MB/s)

Signal Pin Count

Next Gen Serial?
133MHz x16 AAD Sync
52Mhz x16 Sync
x16 Page Mode
108MHz x8 SPI
108MHz x4 SPI
50MHz x1 SPI

* Bubble size shows BW/pin
Summary

- It’s happening today
- Driving system complexity and memory growth
  - Including NAND and DRAM
- Performance and Security growing needs that NOR memory can fill
  - SPI, Advanced Parallel and future SPI architectures

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