



Optimizing Top Level Signal Planning for Flash Memory

Bob Eisenstadt
Senior Technologist, Pulsic Inc.

Overview

- Pulsic and Precision Design Automation
- Flash Memory Signal Planning Challenges
- Spine Routing for Extreme Aspect Ratio Channels
- Automating and Optimizing Block Pin Placement
- Summary

Precision Design Automation

- About Pulsic
 - Pulsic is an EDA company founded in 2000
 - Customers include 7 of 10 largest memory suppliers
 - HQ in Bristol UK, plus offices in San Jose and Tokyo
 - Physical Design Solutions for Custom and AMS IC's

- Precision Design Automation is needed when:
 - Manual design efforts reach the breaking point
 - Traditional digital design automation tools fall short
 - Hand crafted quality is required



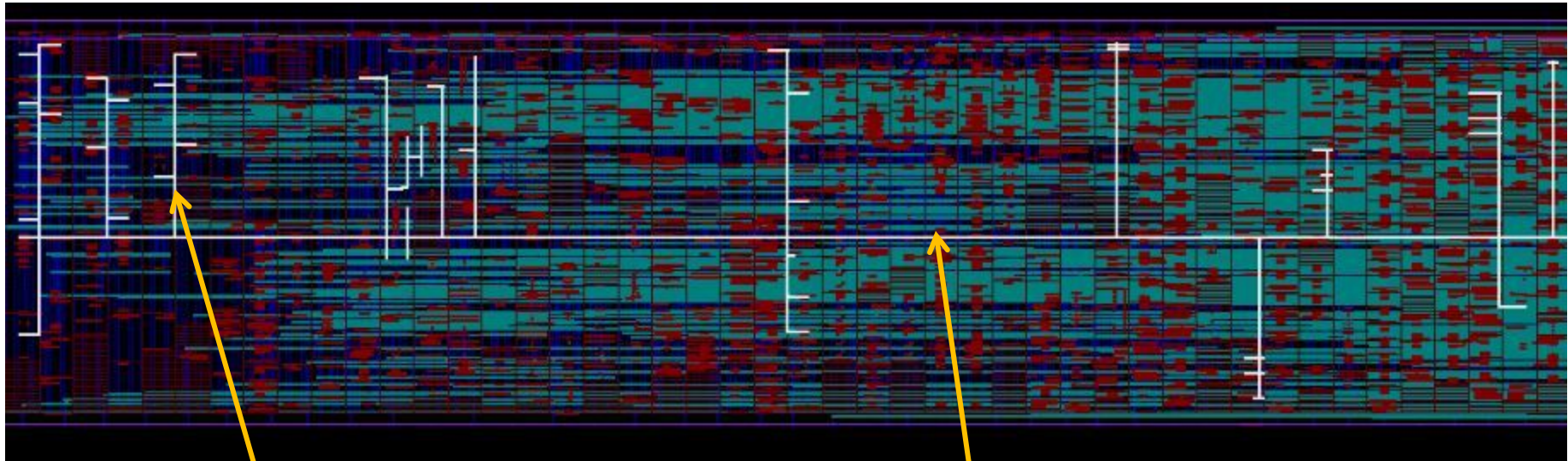
Flash Signal Planning Challenges

- Flash Memory has large arrays and extreme aspect ratio channels with peripheral logic and interfaces.
- Flash has few routing layers, die size minimization is essential, so every routing track counts.
- Design complexity, layout effort, and design rule complexity are always increasing. Meanwhile, design schedules are always shrinking.
- Solution: increase design automation efforts

Spine and Stitch Routing

- Developed primarily for memory designs, which have large arrays with extreme aspect ratio channels that contain cells.
- Channel Router makes straight spine routes in the routing resource limited direction. Then perpendicular stitch routes plus vias connect from the spine routes to cells.
- This optimizes critical routing resource usage, and minimizes channel size and die size.

Spine and Stitch Routing Example



Stitch Route

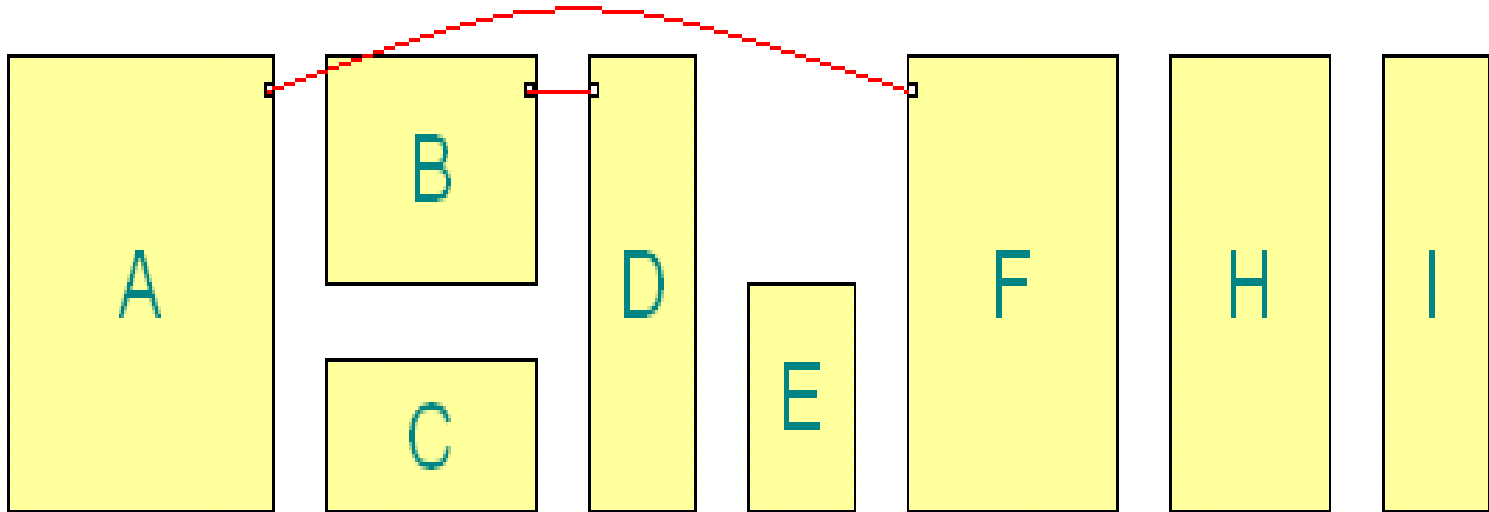
Spine Route

- 1 Horizontal metal layer = Spine routes
- 1 Vertical metal layer = Stitch routes
- Small horizontal stubs = High resistance jumpers

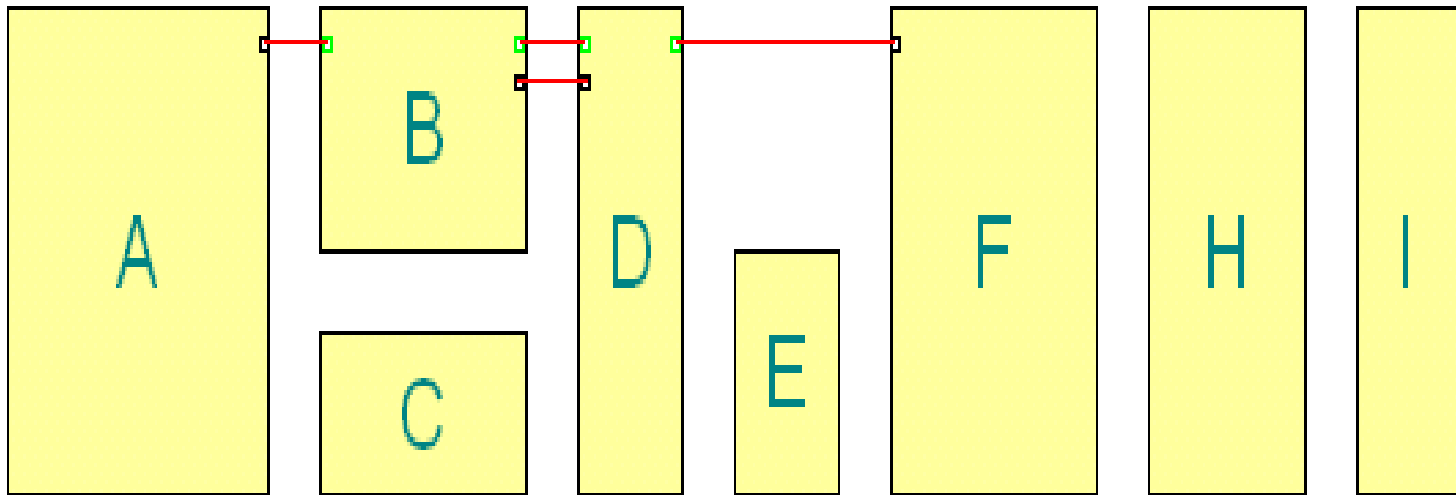
Automating Block Pin Placement

- Complex Flash designs have blocks in their channels requiring optimized pin placement.
- Use Channel Router spine routes to drive the block pin placement, and optimize routing resource usage.
- Once automated block pin placement is done...
 - Push down block pins and feed-throughs into blocks
 - Complete top level channel routing with block abstracts
 - Complete stand alone block level physical design
 - Reintegrate routed blocks with top level

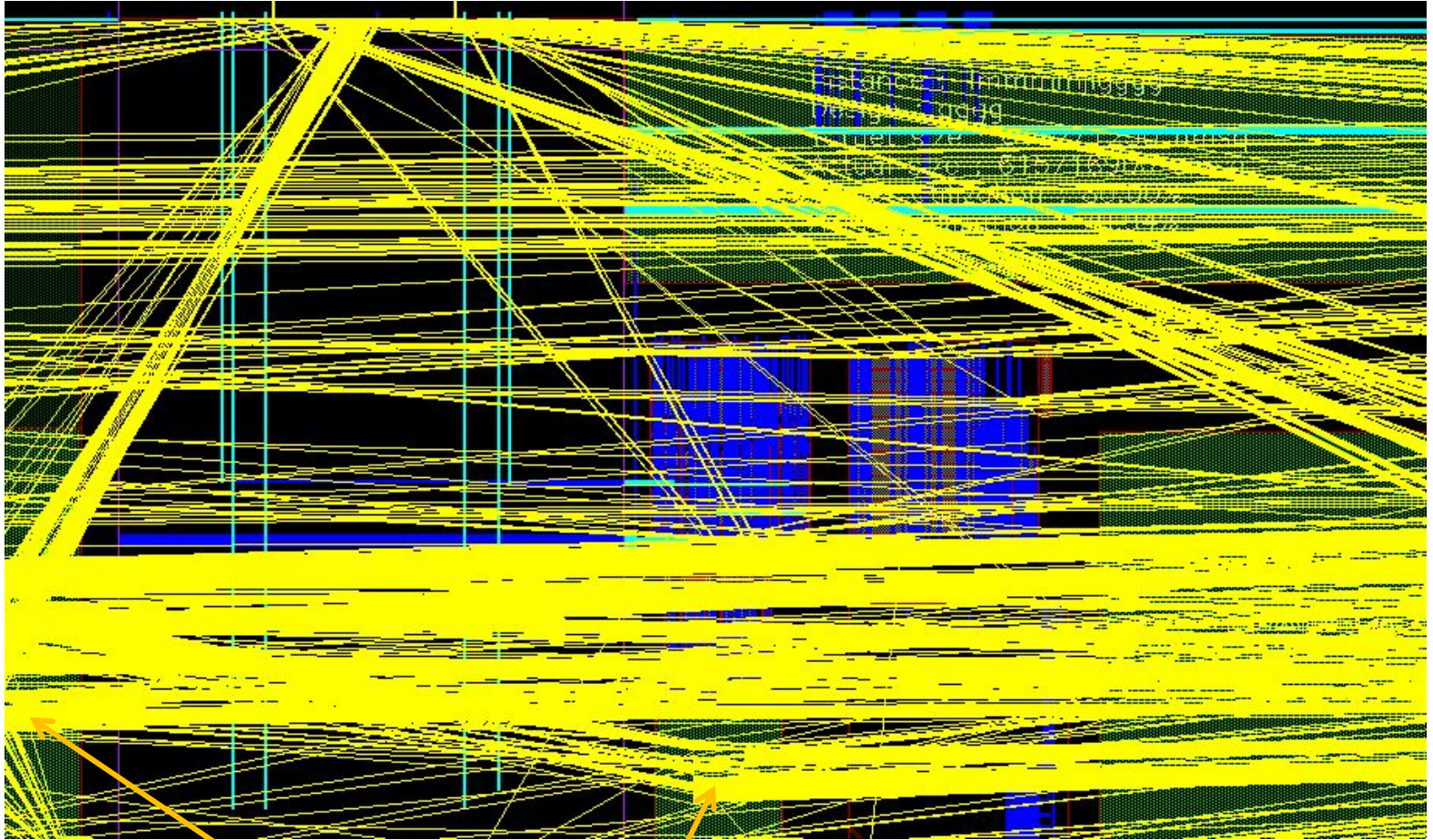
Pin placer aligns pins between blocks but...



Channel Router needs to drive pin placement



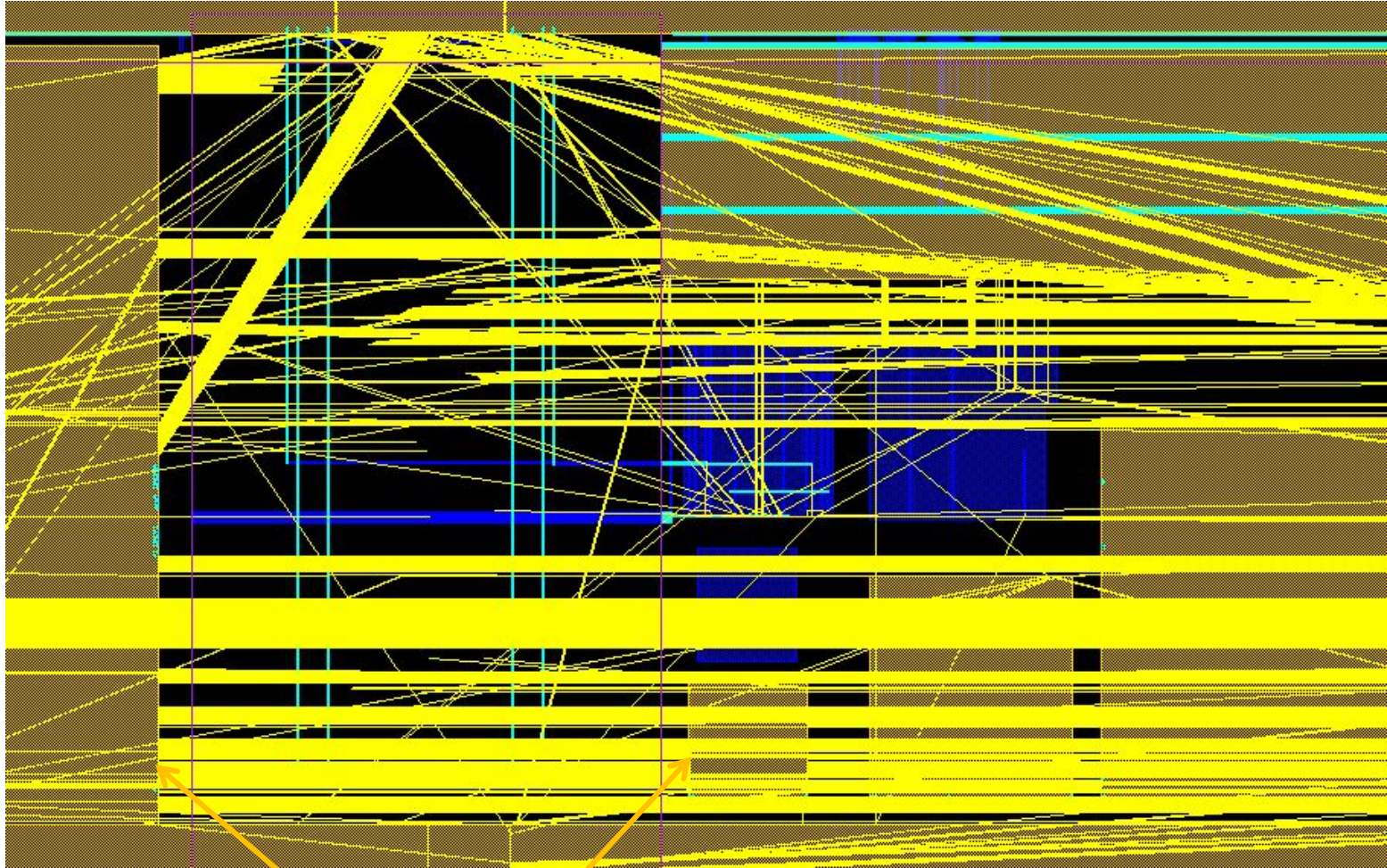
Fly Lines for Blocks Before Automated Pin Placement



Example soft blocks with
unplaced pins in center

Fly lines in Yellow

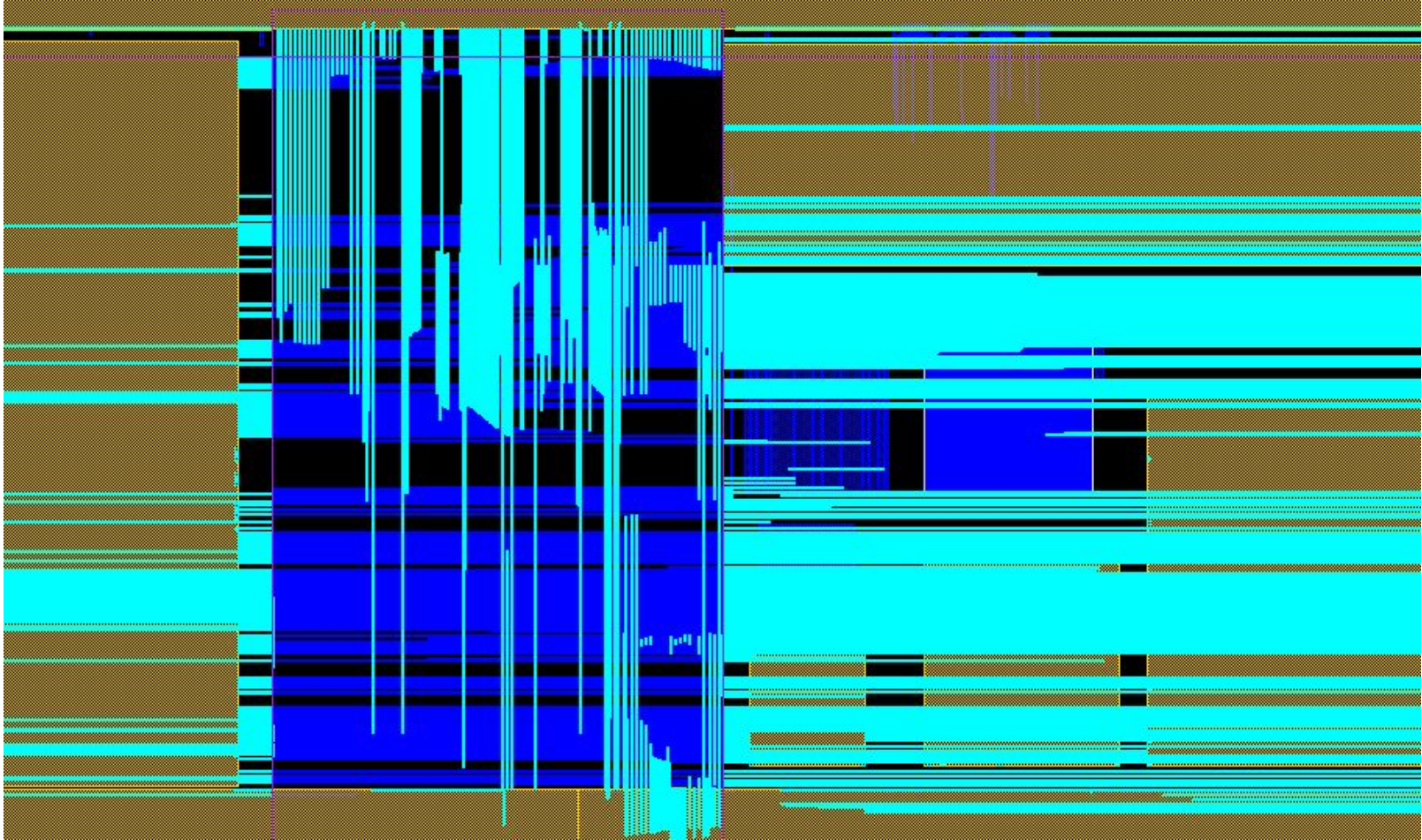
Fly Lines for Blocks After Automated Pin Placement



Example soft blocks with placed pins along edges

Signals Routed in Channel

(power and ground removed to improve visibility)

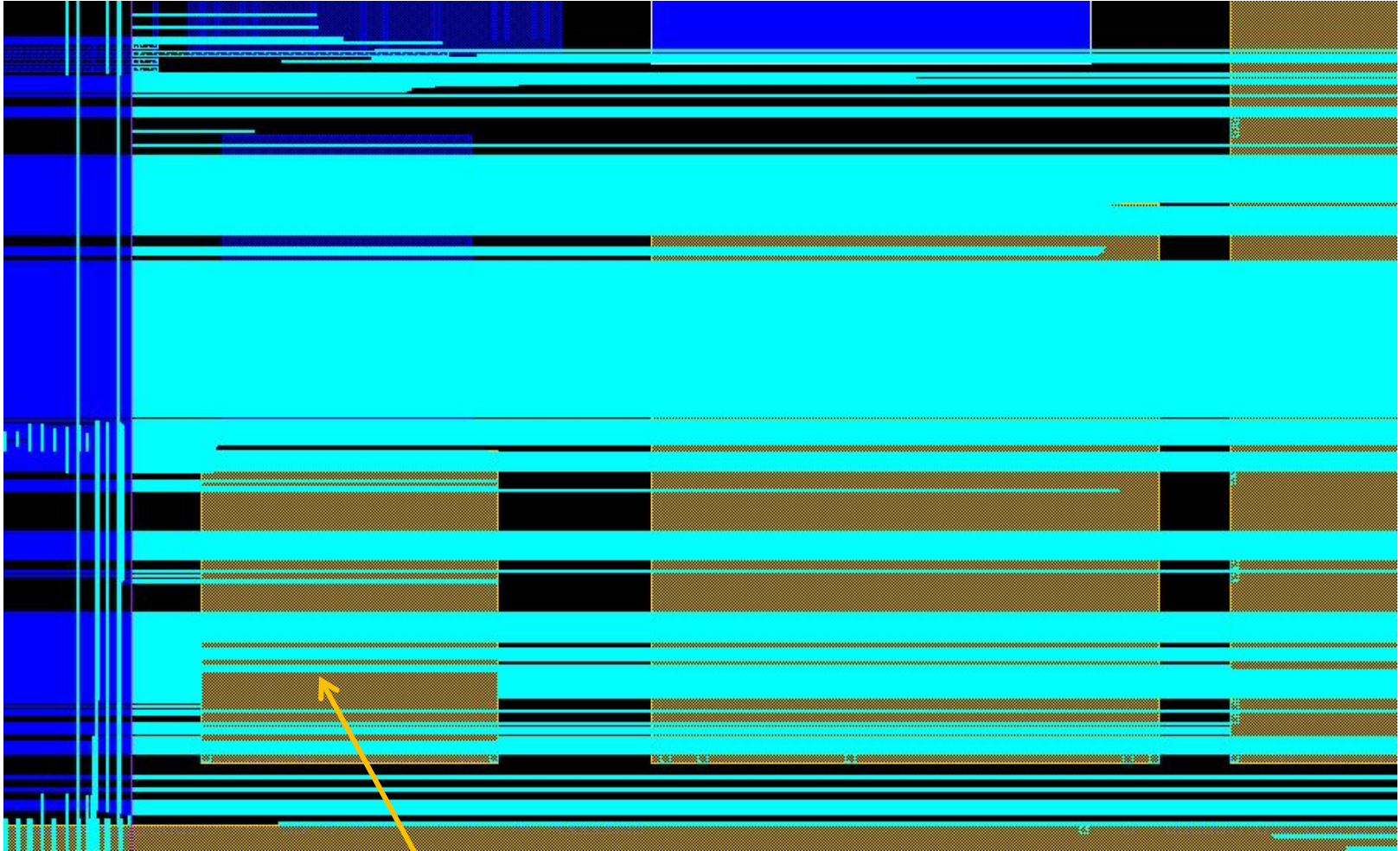


Metal 2 uses multi-biased
routing (X and Y directions)

Metal 1 = Dark Blue
Metal 2 = Light Blue

Routed Blocks

(close up bottom right area)



Example block with pins along edges plus routing feed throughs

Summary

- For extreme aspect ratio channels that contain cells, use a Channel Router to do the Spine and Stitch routing.

- For extreme aspect ratio channels containing blocks, use a Channel Router to automate block level pin placements.
 - Push pins and feed-throughs into the blocks
 - Complete top level routing using block abstracts
 - Complete stand alone block level physical design
 - Reintegrate routed blocks into top level



For Further Information

- www.pulsic.com
- Pulsic 2025 Gateway Place, Suite 350
San Jose, CA 95110
- bob.eisenstadt@pulsic.com
- 408-550-2761 (technical)
- dave.noble@pulsic.com
- 408-550-2760 (business)